

Table of Contents

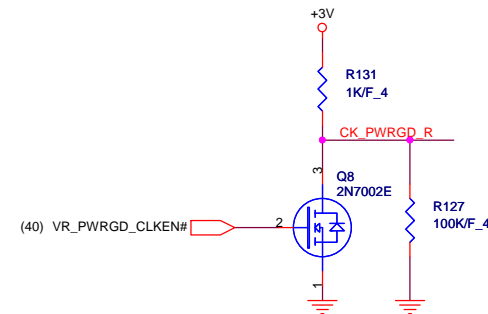
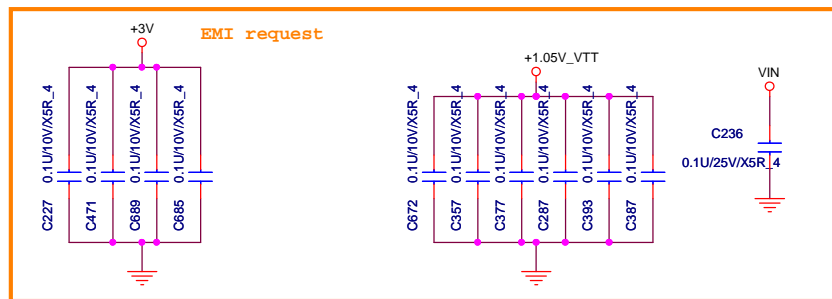
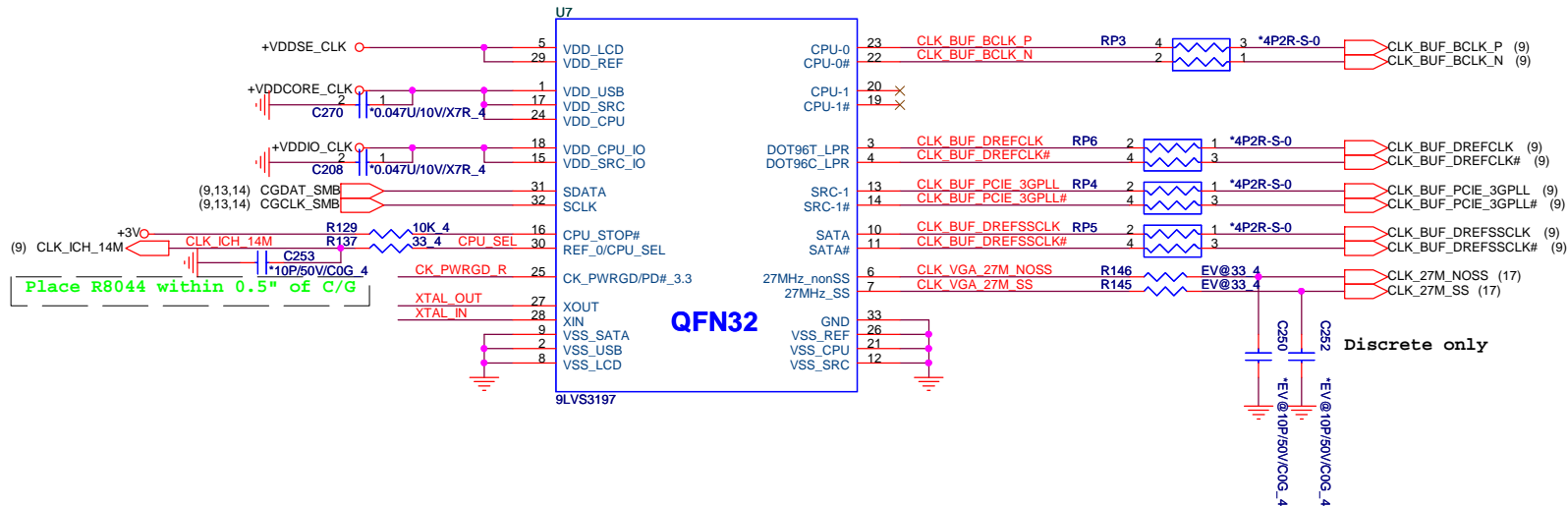
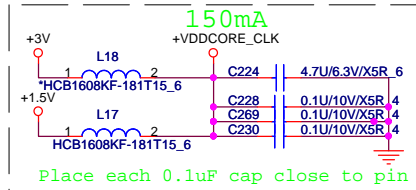
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	CLOCK GENERATOR
4-7	Arrandale CPU
8-12	Ibex Peak-M
13-14	DDRIII SO-DIMM
15-19	Discrete VGA (N11M-GE2)
20	LCD + Camera Conn.
21	CRT Conn.
22	HDMI Conn.
23	ATHEROS (AR8151/AR8152)
24	CARD READER(OZ600FJ)
25	AL272/AMP/MIC/SPK
26	USB x 2 /USB+ ESATA
27	USB X2/SIM_CARD/LEDs/RF
28	MINI-Card (WLAN)
29	MINI-Card ( WWAN/SSD)
33	ONFI
34	Express Card
35	K/B & T/P
36	BLUETOOTH
37	FAN & Thermal
38	G-Sensor
39	B To B Conn.
40	ITPM & RFID EEPROM
41	KBC IT8502E
42	HOLD & SKEW
43	Discharge
44	Charger
45	DDR3 (TPS5116REGR)
46	1.05V_VTT & 1.05_PCH (RT8204)
47	3V/5V (MAX17101)
48	CPU (MAX17082)
49	DIS GFX_VCC (MAX8792)
50	DIS_1.8V_RUN (OZ8116LN)
51	Power Block Diagram
52	XDP
53	Revision & Schematic Value Description
54	BOM Matrix Table

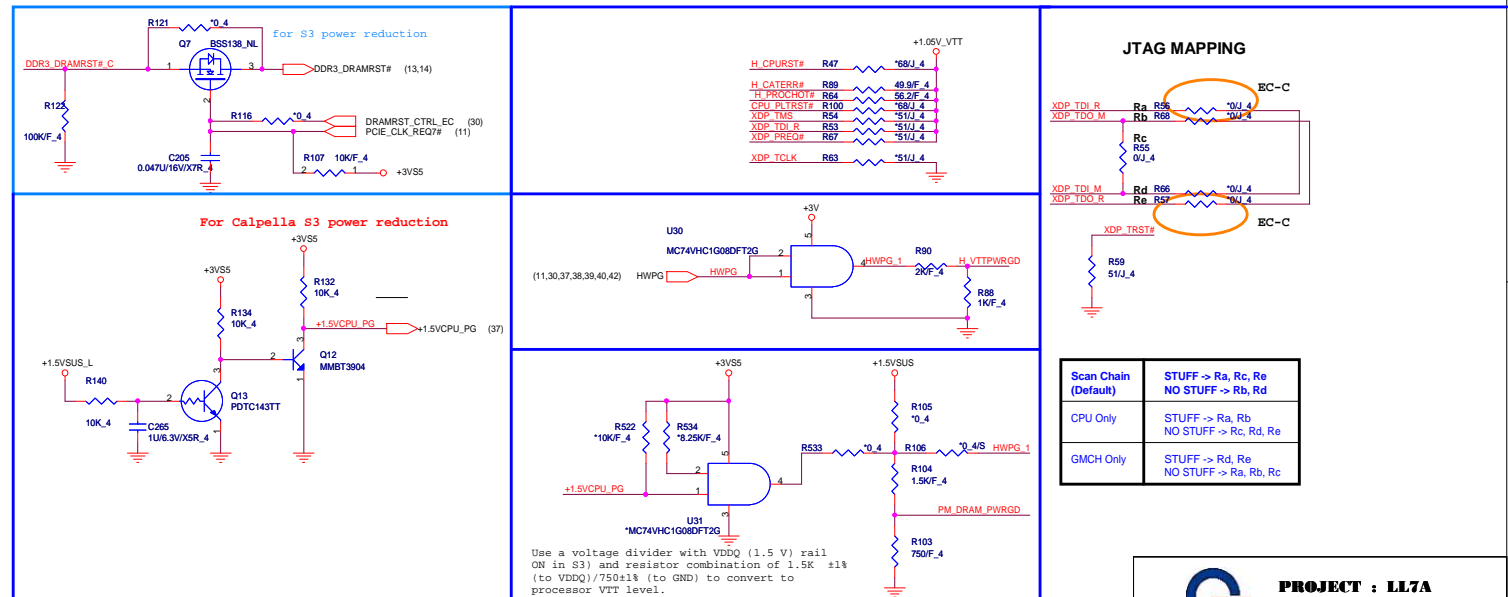
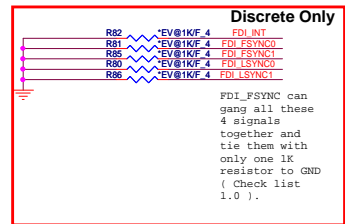
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0-S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0-S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0-S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0-S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WIMAX POWER	S5_ON	S0-S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0-S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0-S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0-S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0-S5



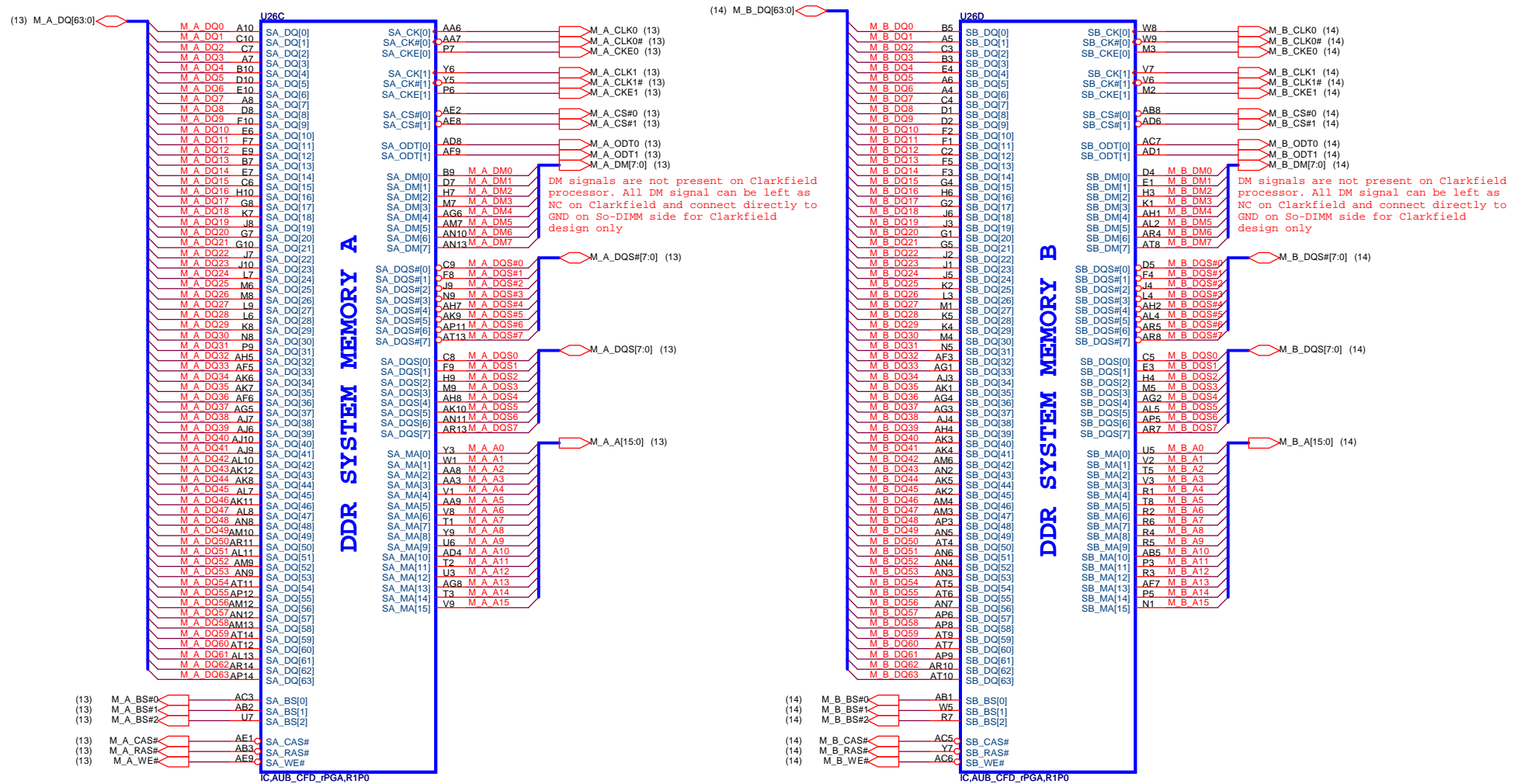
**PROJECT : LL7A**  
**Quanta Computer Inc.**



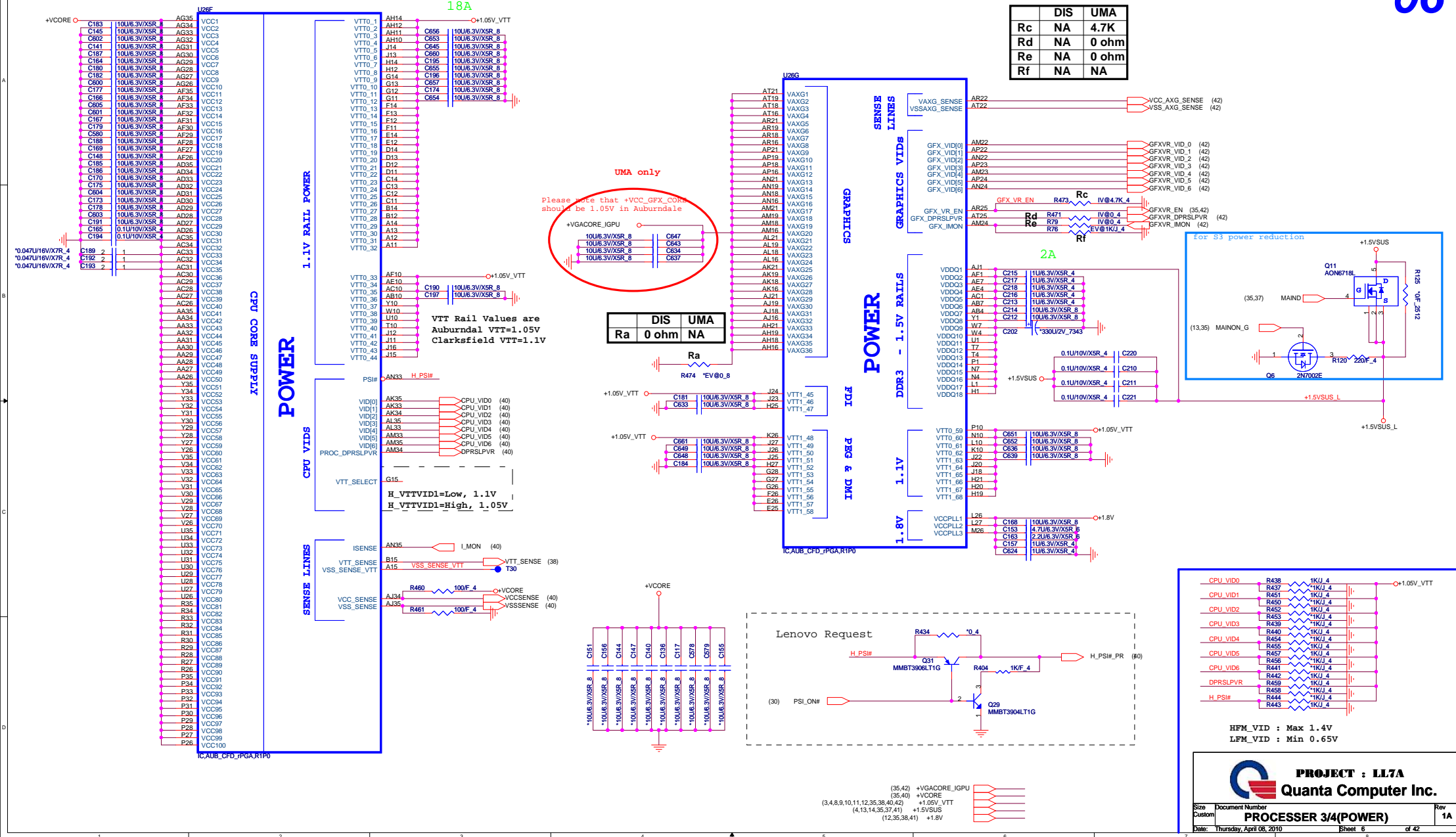


Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

## AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

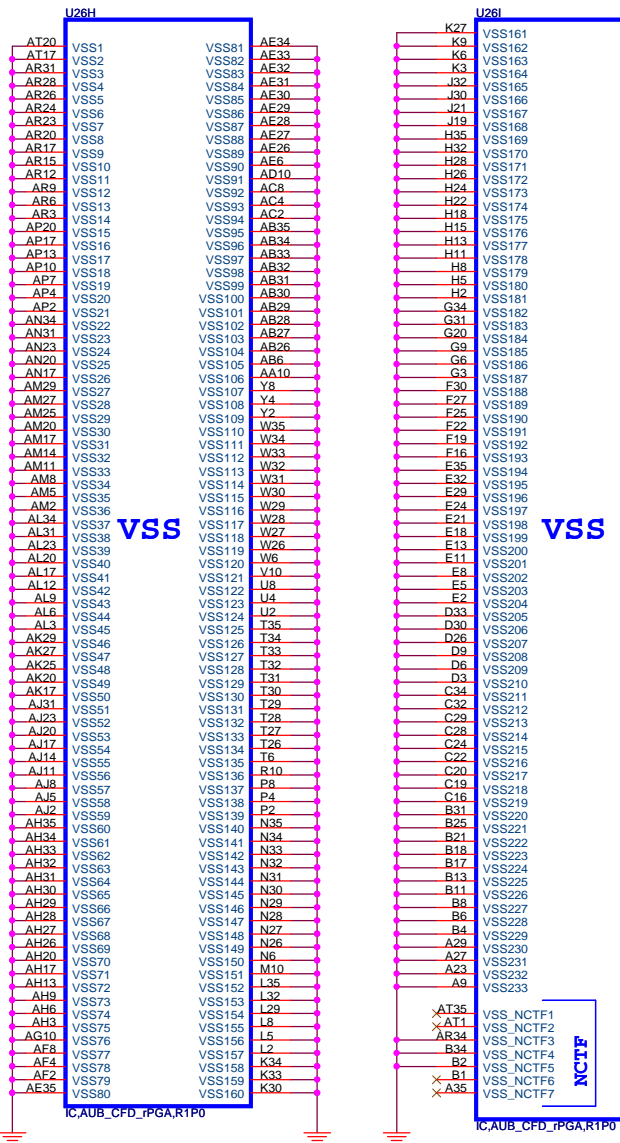


**PROJECT : LL7A**  
**Quanta Computer Inc.**

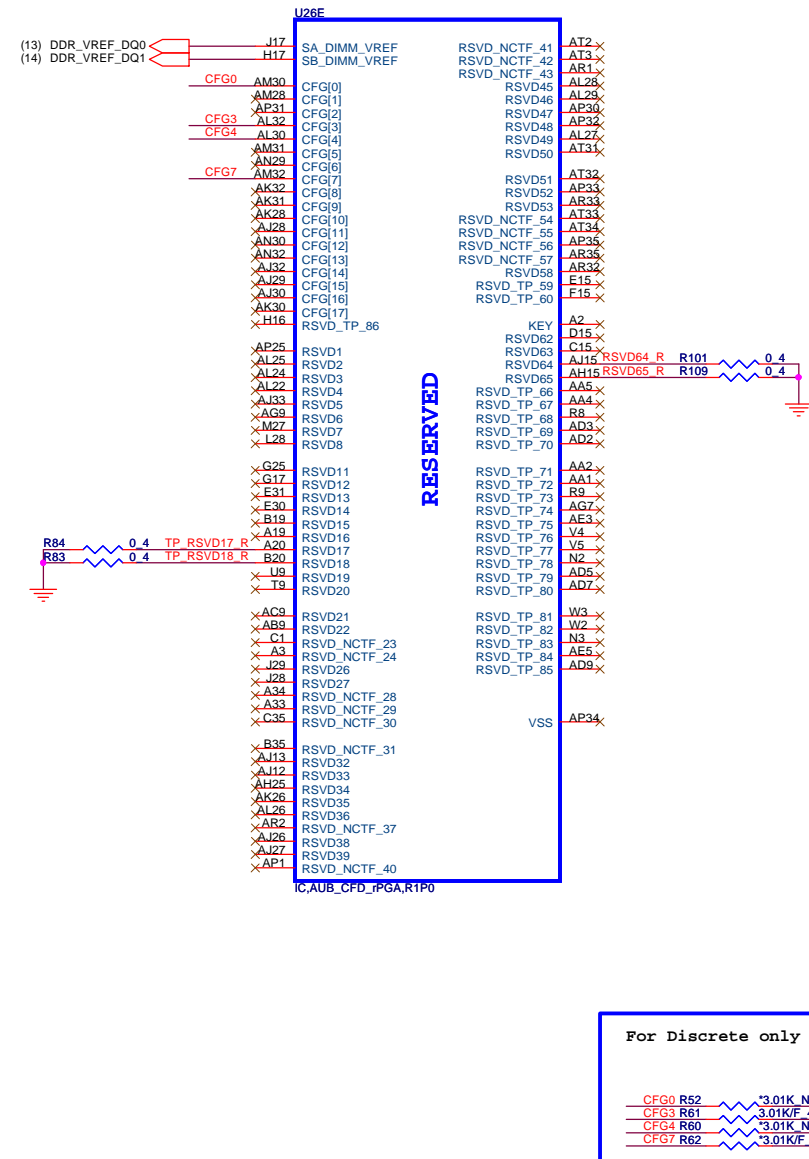




AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



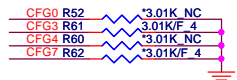
AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

For Discrete only



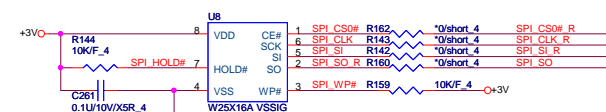
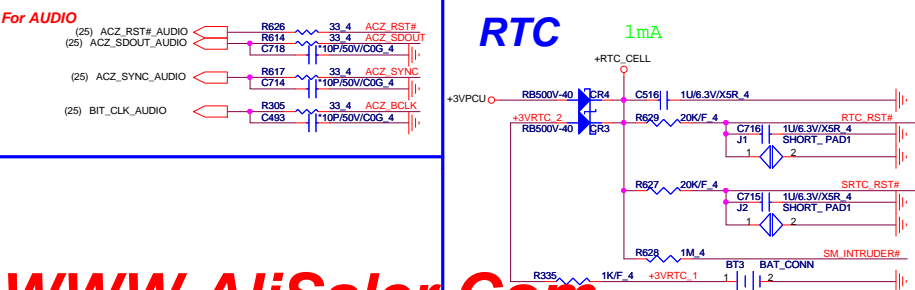
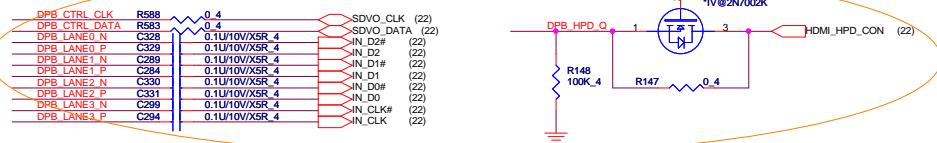
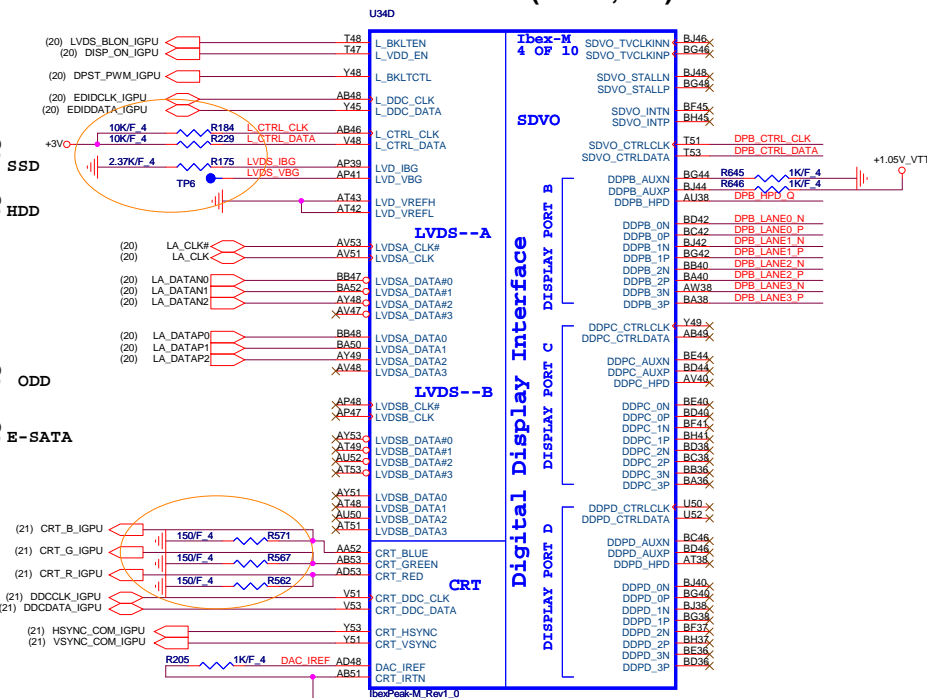
CFG[ 1:0 ] - PCI\_Epress Configuration Select  
\* 11= 1 x 16 PEG  
\* 10= 2 x 8 PEG



**PROJECT : LL7A**  
**Quanta Computer Inc.**

Size: Custom  
Document Number: **PROCESSER 4/4(GND)**  
Date: Thursday, April 08, 2010  
Sheet 7 of 42

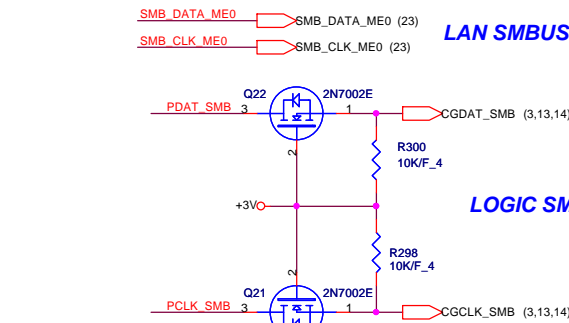
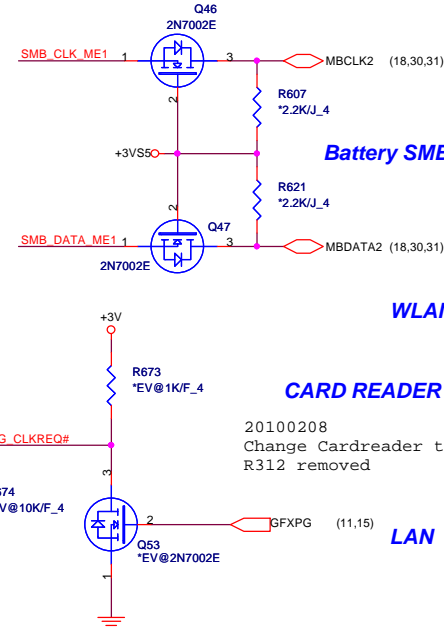
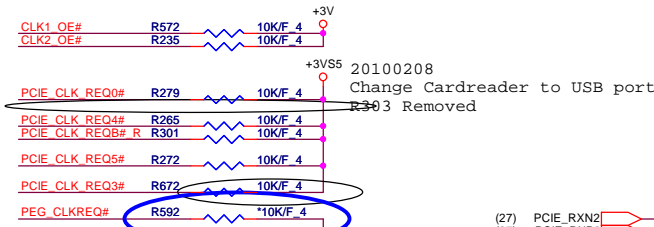
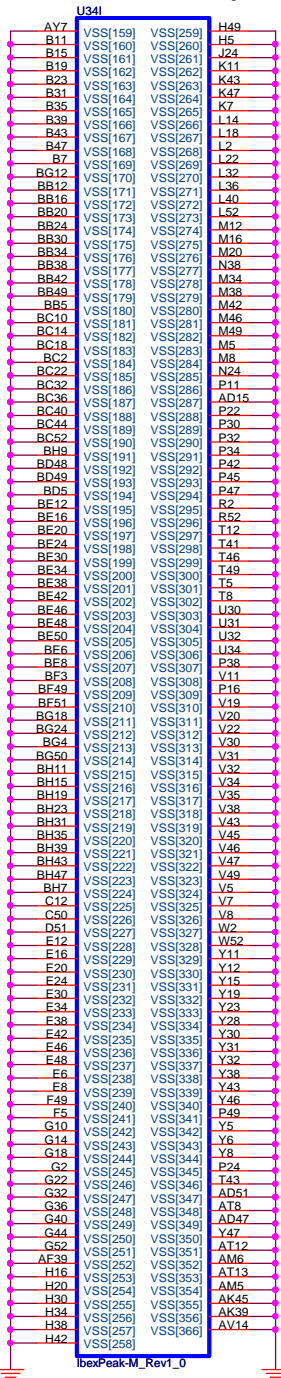
Rev: 1A



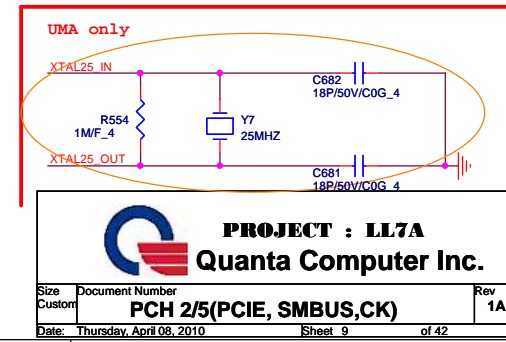
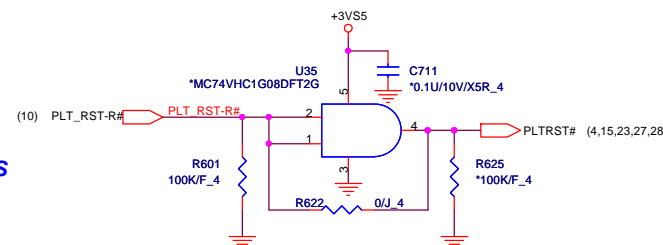
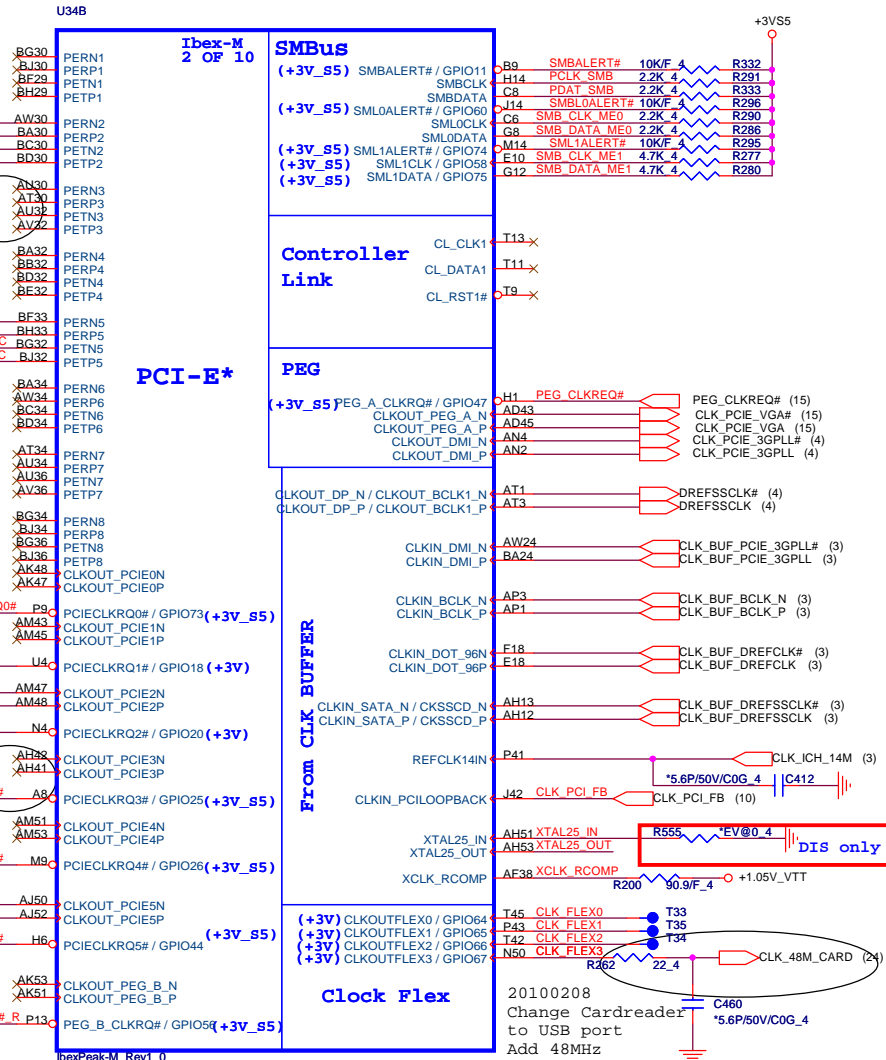
Vendor	PN
Socket	DG008000031
WINBOND	AKE39ZP0N00
MAX	AKE39FP0N00



## IBEX PEAK-M (GND)



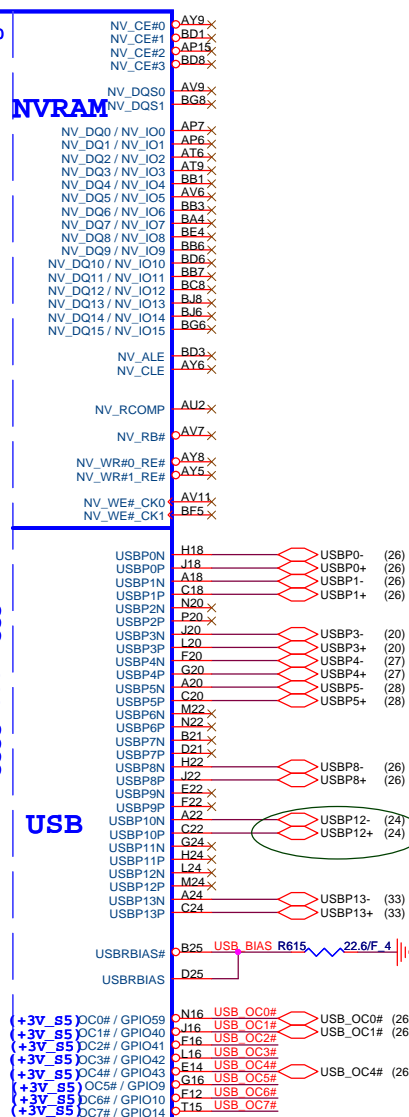
## IBEX PEAK-M (PCI-E, SMBUS, CLK)



(4,8,10,11,12,15,27,35) +3V55  
(3,4,6,8,10,11,12,35,38,40,42) +1.05V\_VTT  
(3,4,8,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V

U34E

X H40	AD0	Ibex-M
X N34	AD1	5 OF 10



**LEFT SIDE USB 0**

**LEFT SIDE USB 1**

**CCD**

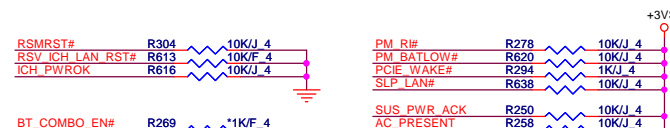
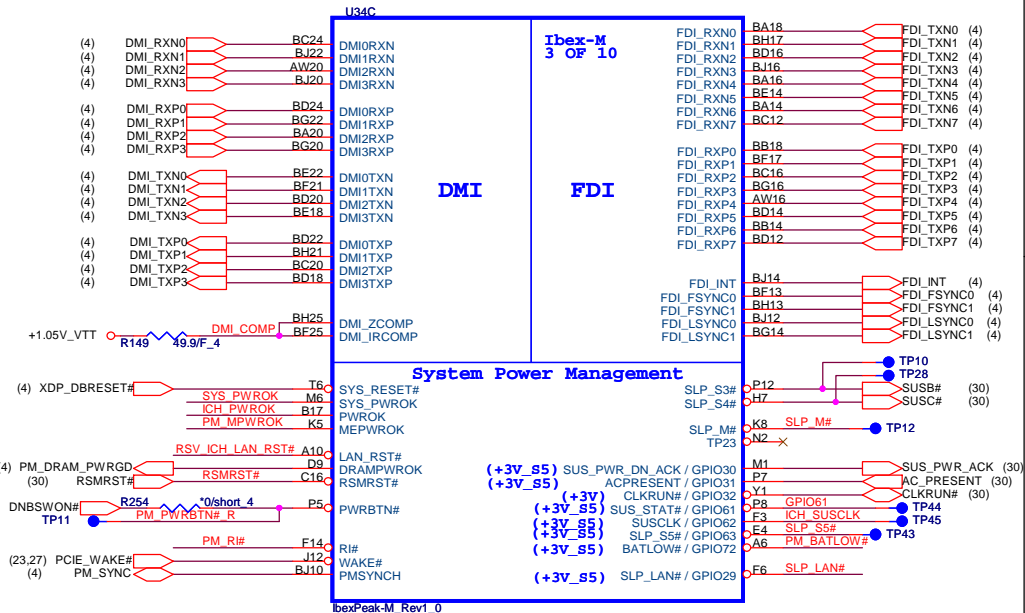
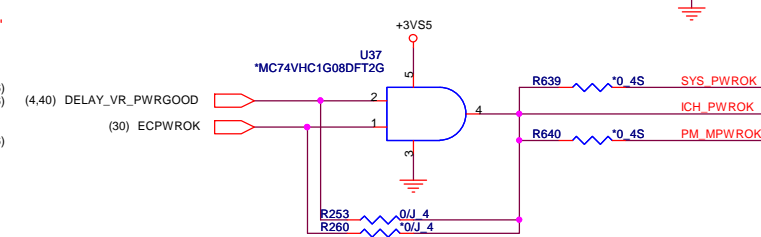
## WLAN

## WWAN

**LEFT SIDE USB 3**

**Card Reader**

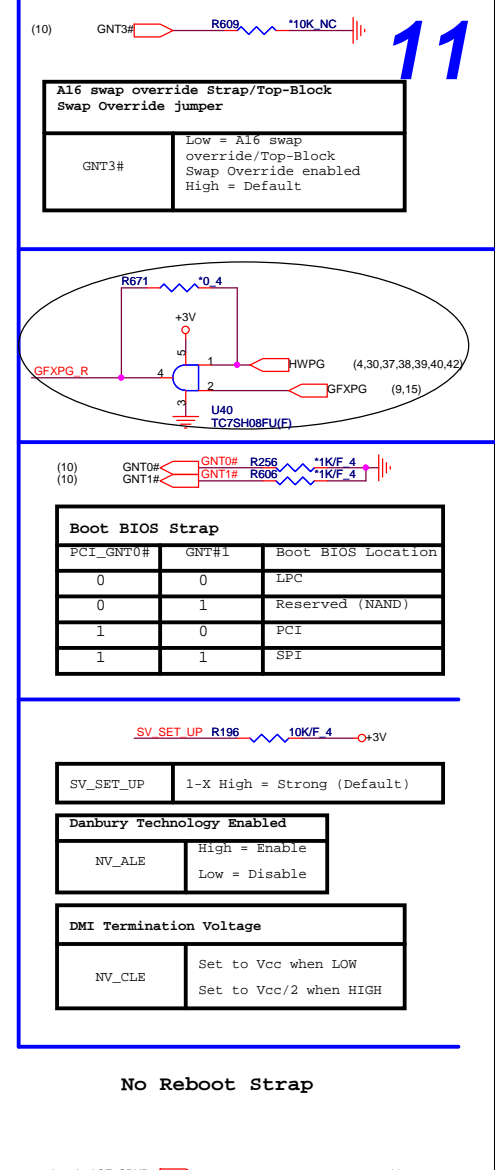
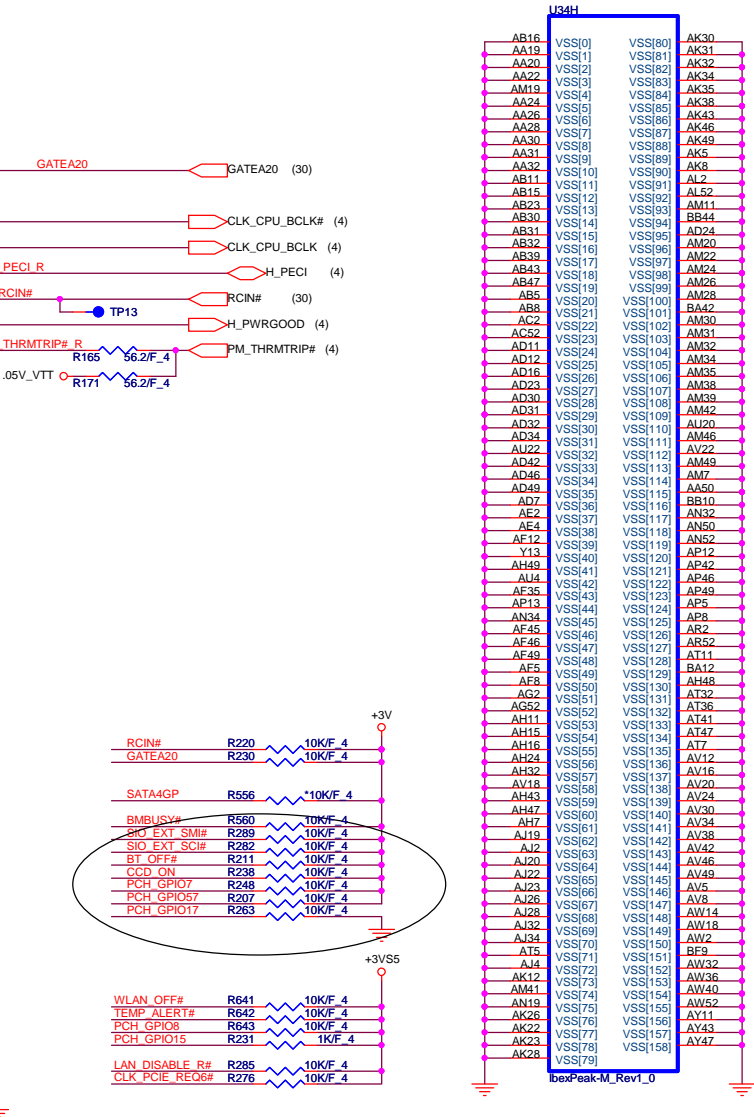
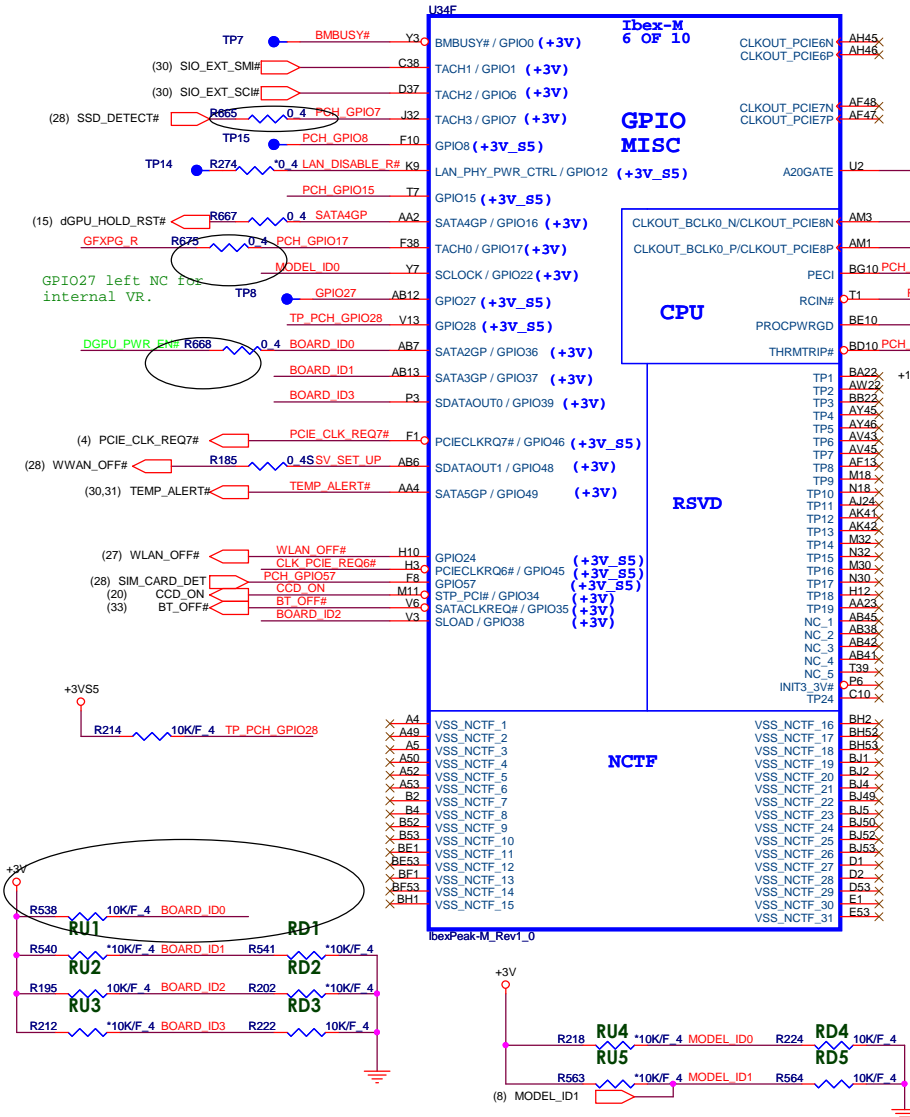
## Blue tooth



# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

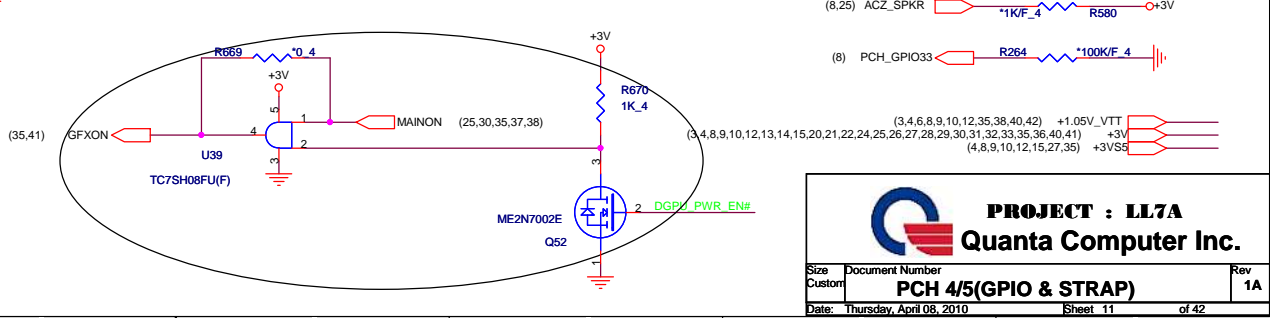
# IBEX PEAK-M (GND)

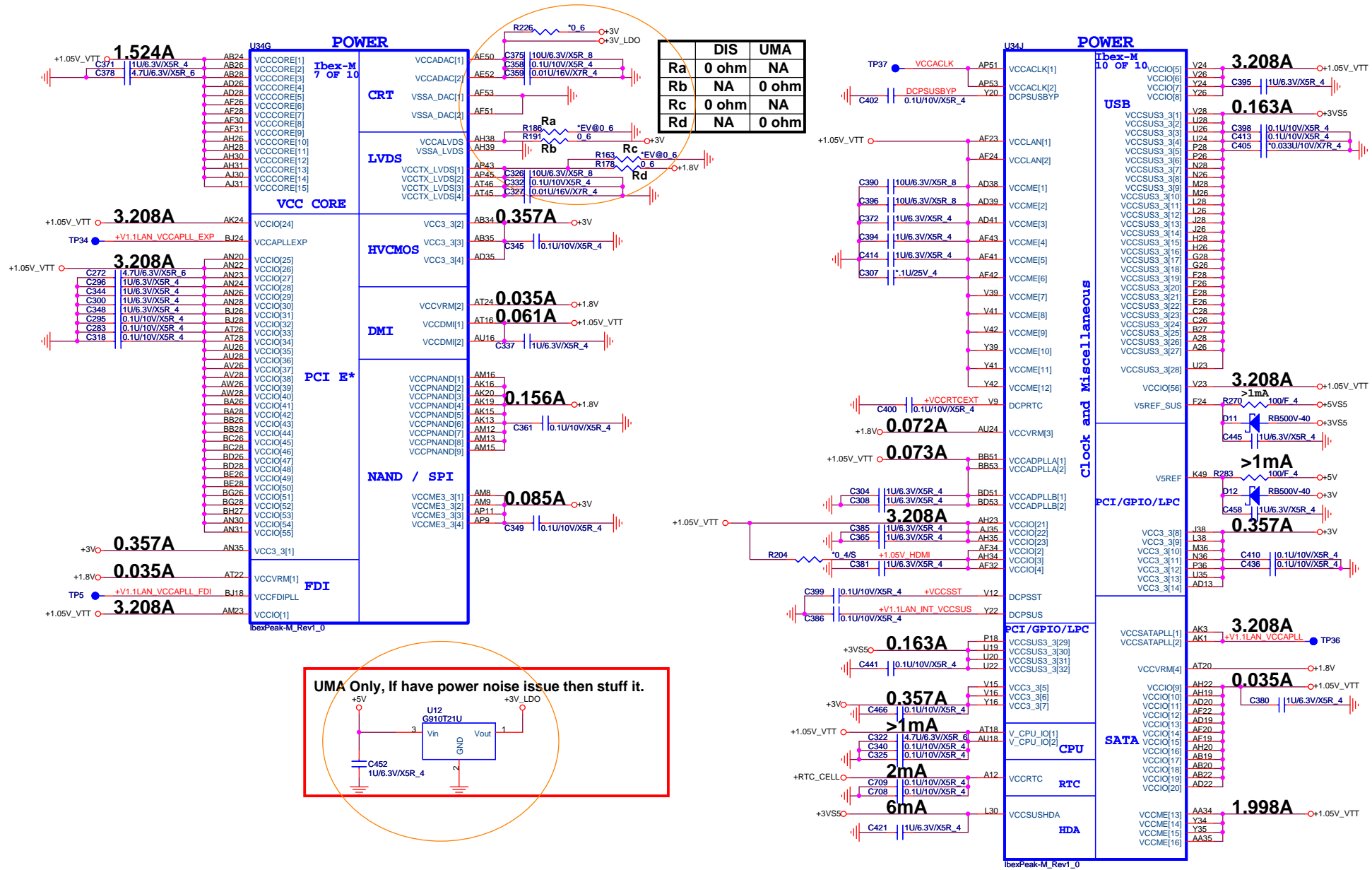
11



Board ID For Function	ID1 GPIO37	ID2 GPIO38	ID3 GPIO39
SDV	0	0	0
SIV	0	0	0
SIT	0	1	0
SVT	1	0	0
SOVP	0	1	0

Model ID	MODEL_ID0	MODEL_ID1
Default	0	0
LL7	0	1
LL7A	1	0





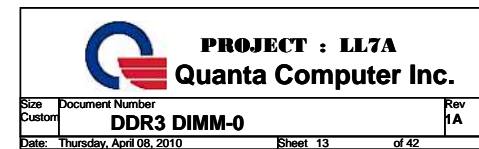
(3,4,6,8,9,10,11,35,38,40,42) +1.05V\_VTT  
(6,35,38,41) +1.8V  
(3,4,8,9,10,11,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V  
(4,8,9,10,11,15,27,35) +3VS5  
(20,21,22,25,29,30,31,32,33,35,36) +5V  
(26,35) +5VS5

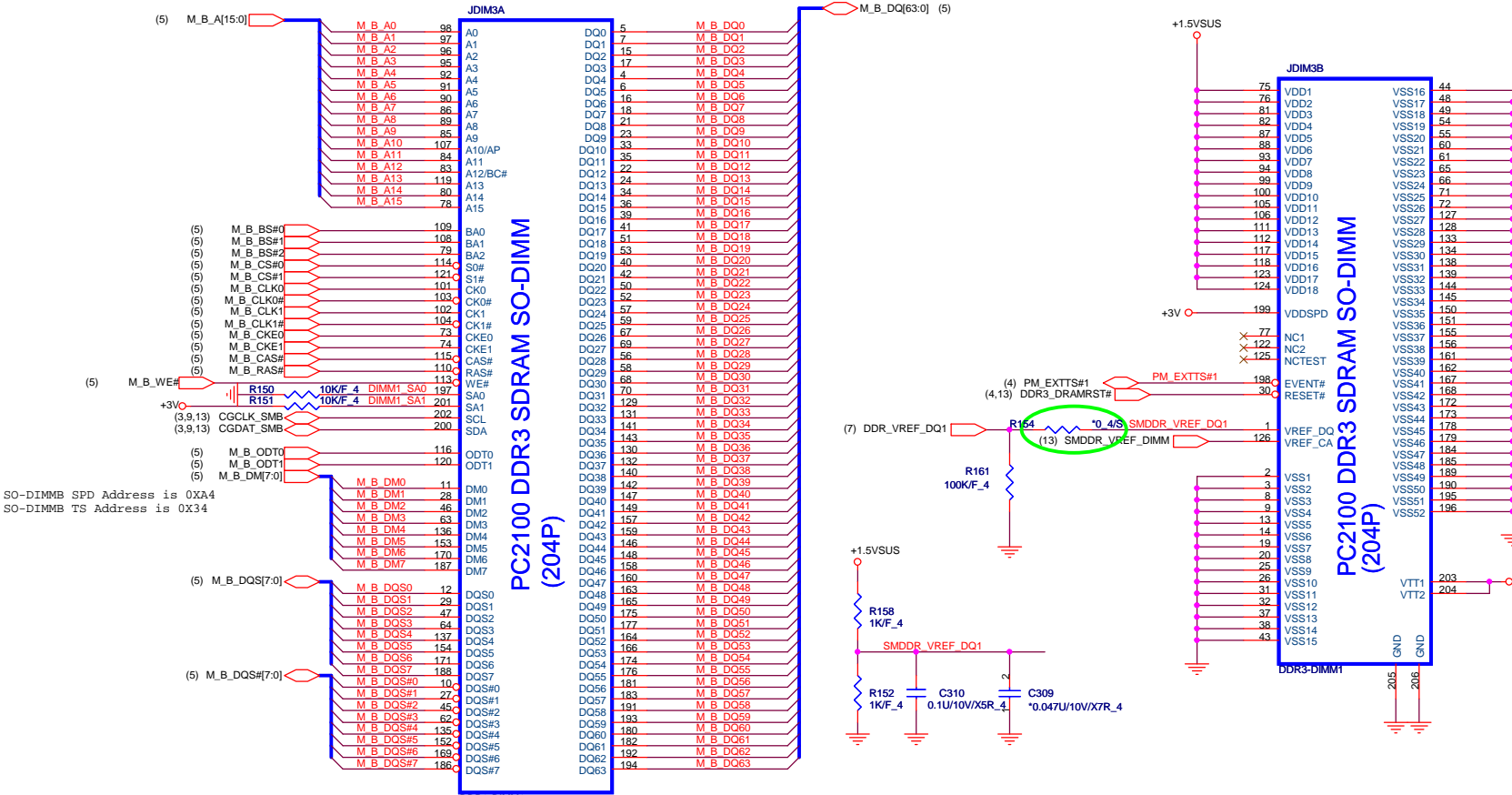


**PROJECT : LL7A**  
**Quanta Computer Inc.**

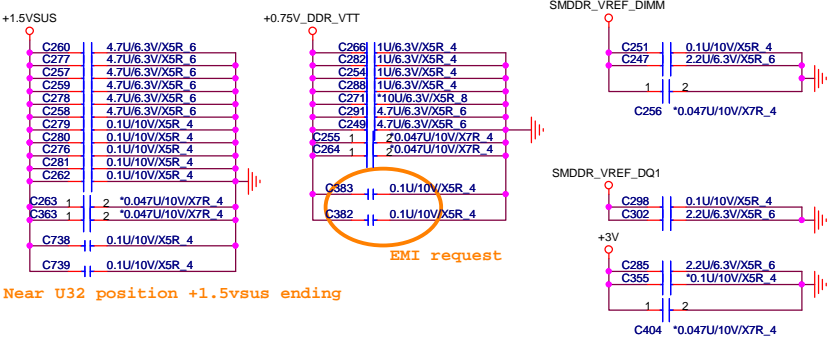
Size: Custom Document Number: PCH 5/5(POWER) Rev 1A  
Date: Thursday, April 08, 2010 Sheet 12 of 42








**Place these Caps near So-Dimm1.**  
 Some Projects replace 10UF 0805 by 4.7UF 0603  
 It can cost down 30%

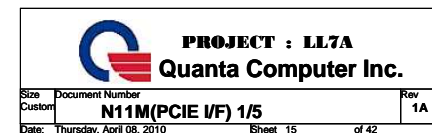
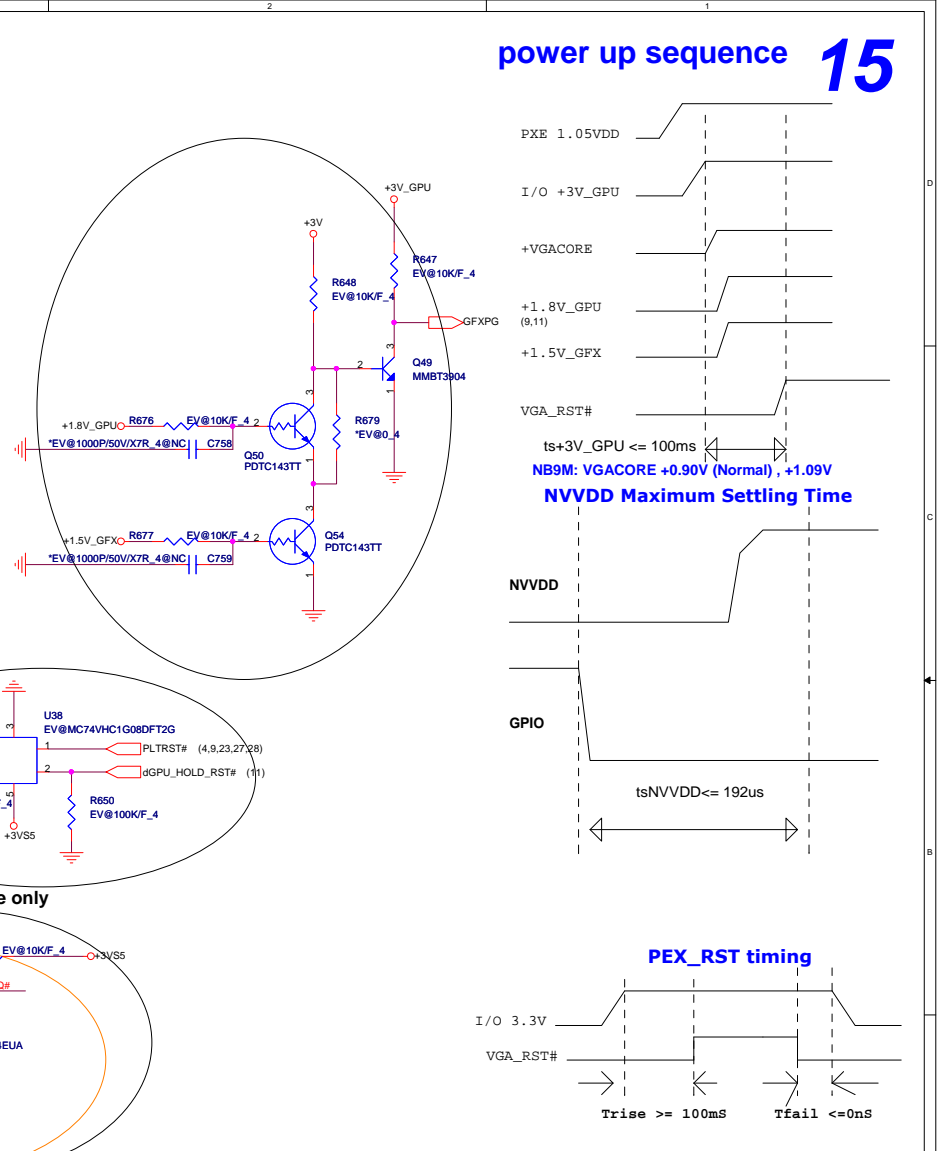




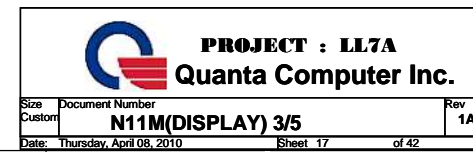
**PROJECT : LL7A**  
**Quanta Computer Inc.**

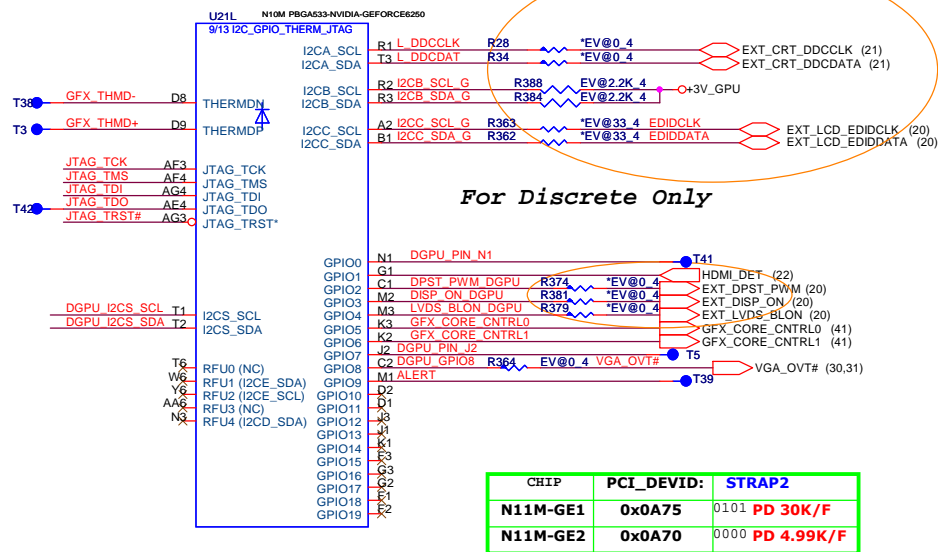
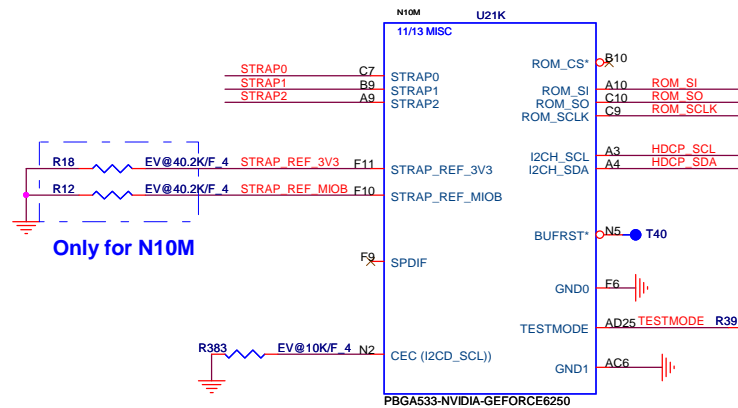
Size	Document Number	Rev
Custom	<b>DDR3 DIMM-1</b>	<b>1A</b>
Date:	Thursday, April 08, 2010	Sheet 14 of 42







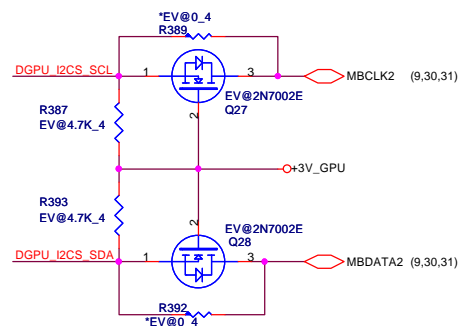




CHIP	PCI_DEVID:	STRAP2
N11M-GE1	0x0A75	0101 PD 30K/F
N11M-GE2	0x0A70	0000 PD 4.99K/F

VRAM Type	RAMCFG[0..3]	ROM_SI
Hynix AKD5LZGTW05	0x0A75	0010 PD15K/F
Samsung AKD5LGGT507	0x0A70	0011 PD 20K/F
Hynix AKD5MGGTW00	0x0A75	0110 PD 34.8K/F
Samsung AKD5MGGT501	0x0A70	0111 PD 45.3K/F

GPU Type	STRAP0	STRAP1	ROM_SO	ROM_SCLK
N11M-GE1	PU 45.3K/F	PU 34.8K/F	PD10K/F	PU15K/F
N11M-GE2	PU 45.3K/F	PU 34.8K/F	PD10K/F	PU15K/F

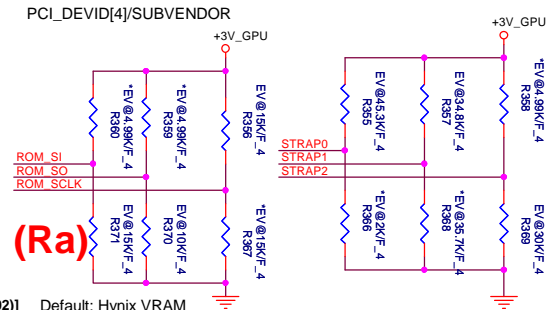


### Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]  
 10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]  
 15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]  
 30K/F 4: CS33002FB13 [RES CHIP 30K 1/16W +1%(0402)]  
 34.8K/F 4: CS33482FB22 [RES CHIP 34.8K 1/16W +1%(0402)]  
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

SEE Datasheet for details on N10P Straps!



Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

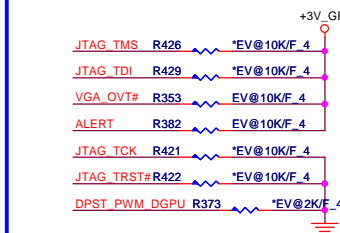
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	Reserved	Reserved		
0001	DDR3 64Mx16x4, 128bit, 512MB, 800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K/F
0010	DDR3 64Mx16x4, 128bit, 512MB, 800MHz	Samsung	K4W1G1646E-HC12	PD 20K/F
0011	Reserved	Reserved		
0101	DDR3 128Mx16x4, 128bit, 1GB, 800MHz	Hynix	H5TQ2G63BFR-12C	PD 34.8K/F
0110	DDR3 128Mx16x4, 128bit, 1GB, 800MHz	Samsung	K4W2G1646E-HC12	PD 45.3K/F
0111	Reserved	Reserved		

(Ra)

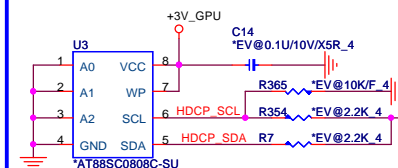
AKD5LZGTW05  
AKD5LGGT507  
AKD5MGGTW00  
AKD5MGGT501

### GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



### HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

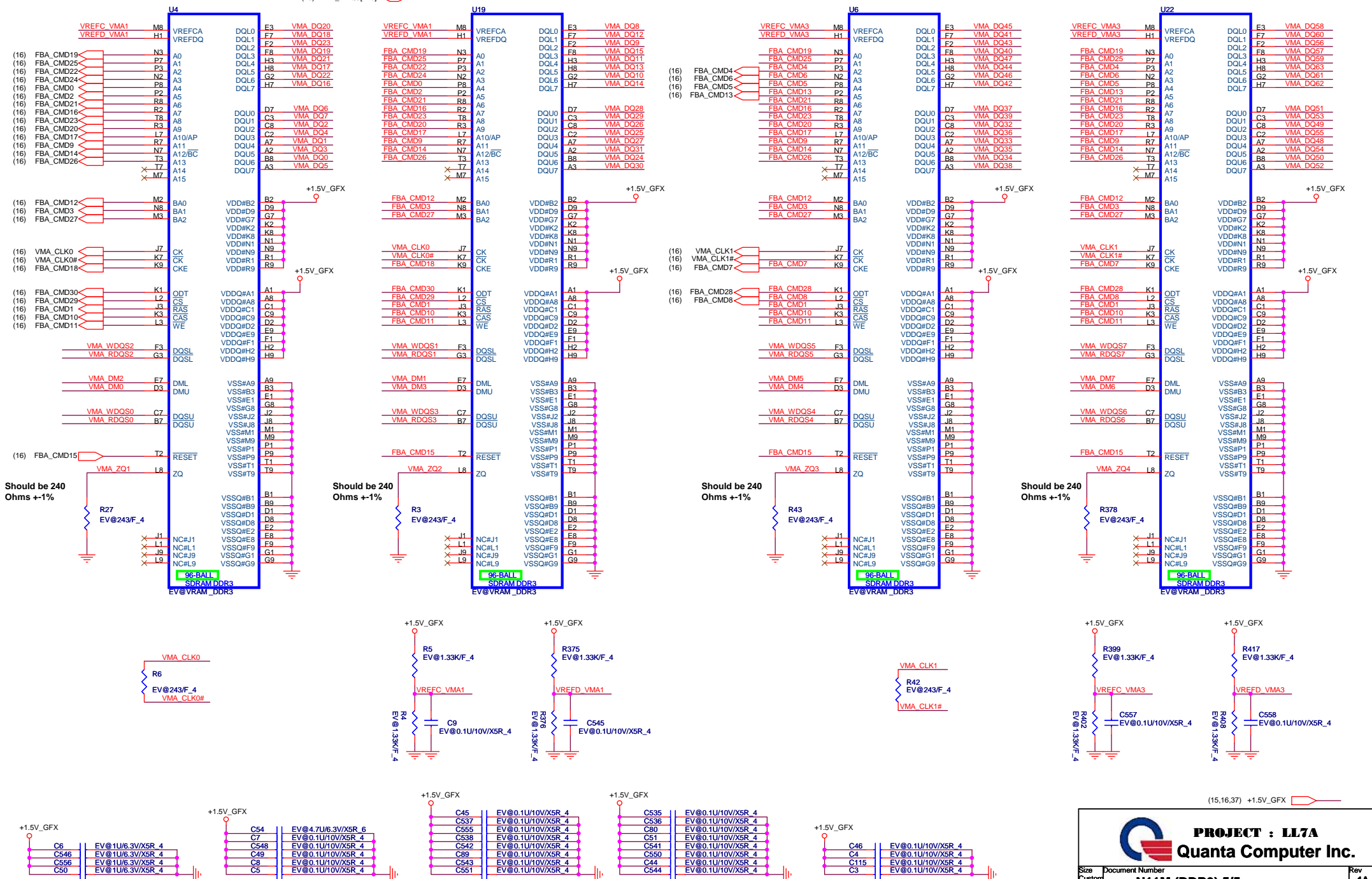


**PROJECT : Z360**  
**Quanta Computer Inc.**

Size: Custom Document Number: N11M(GPIO & STRAPS) 4/5 Rev: 1A  
 Date: Thursday, April 08, 2010 Sheet: 18 of 42

**CHANNEL A: 256MB/512MB DDR3**

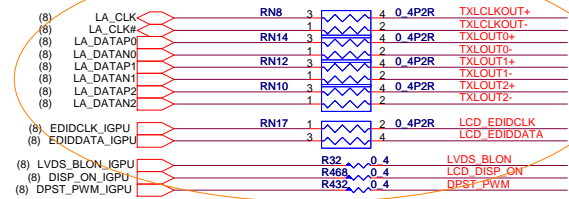
```
(16) VMA_DQ[63..0]
(16) VMA_DM[7..0]
(16) VMA_WDQS[7..0]
(16) VMA_RDQS[7..0]
```



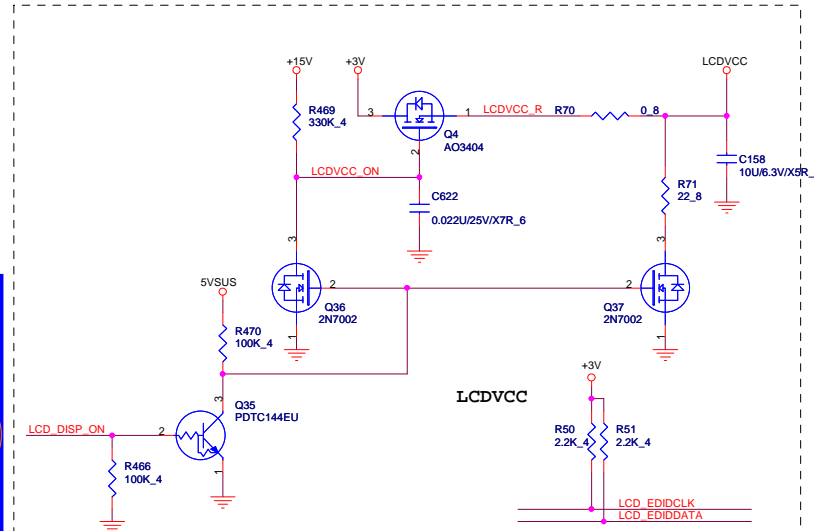
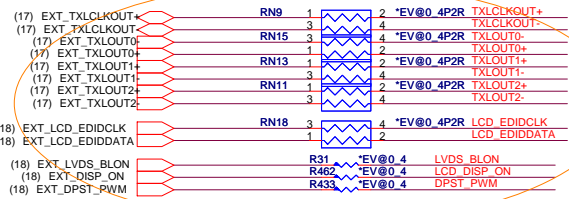


1. If LCD connector near GPU, then place these series Resistors near GPU  
 2. If LCD connector near PCH, then place these series Resistors near PCH

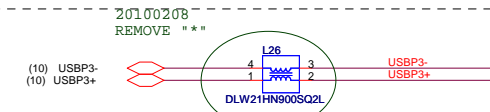
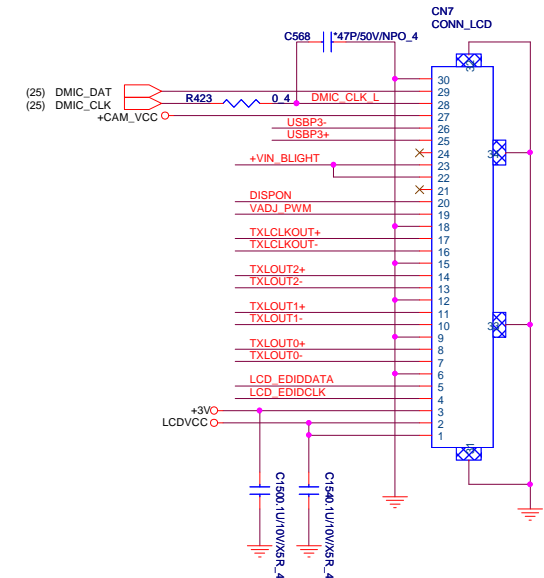
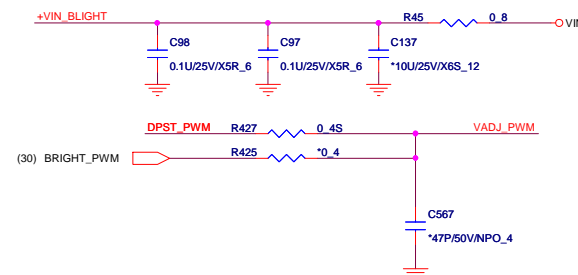
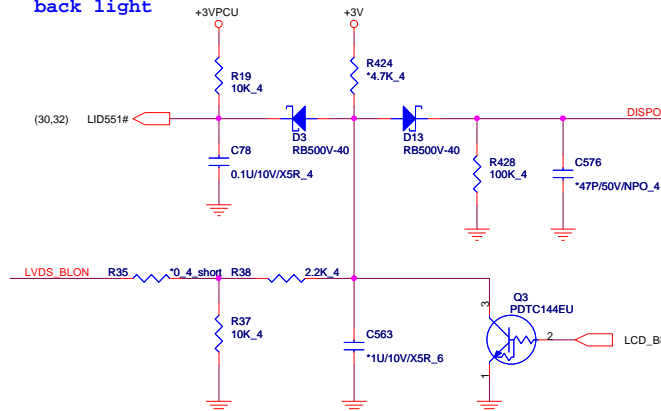
## OPTION SIGNAL FROM PCH FOR UMA VGA



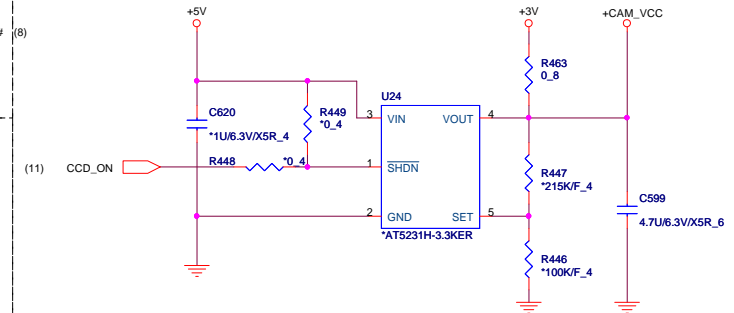
## OPTION SIGNAL FROM N11M-GE2 to VGA



## back light

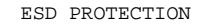


## CAMERA VCC Control



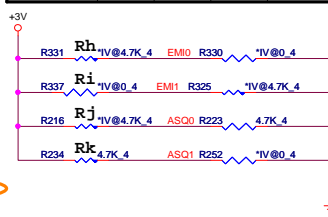
PROJECT : LL7A  
 Quanta Computer Inc.



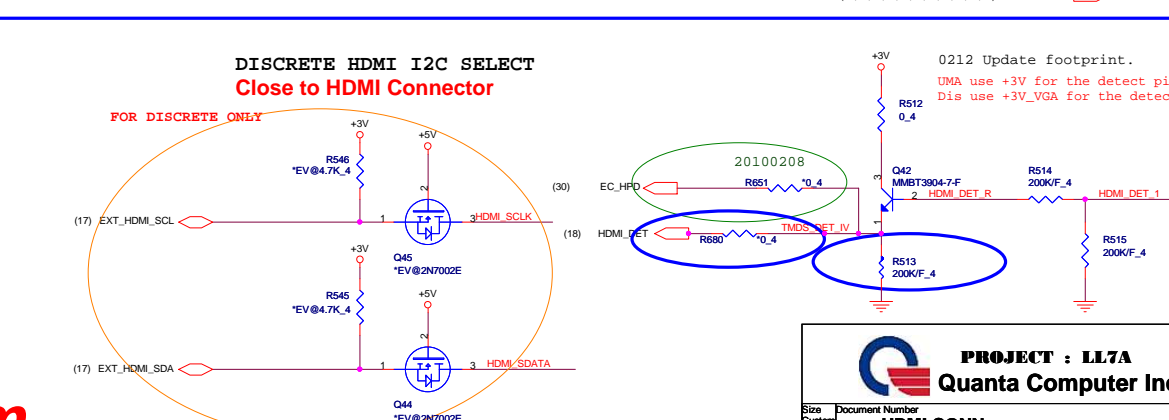
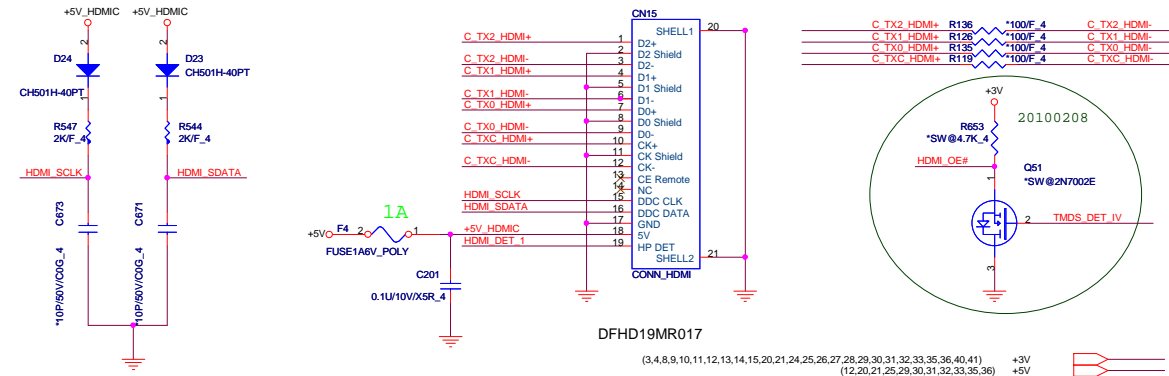
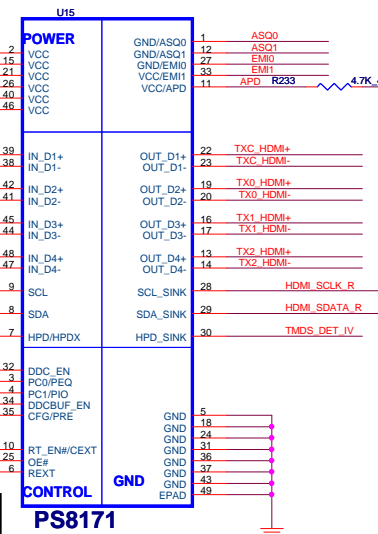


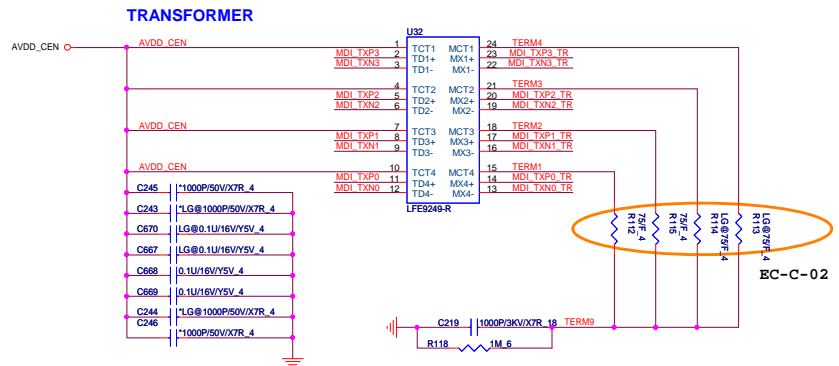
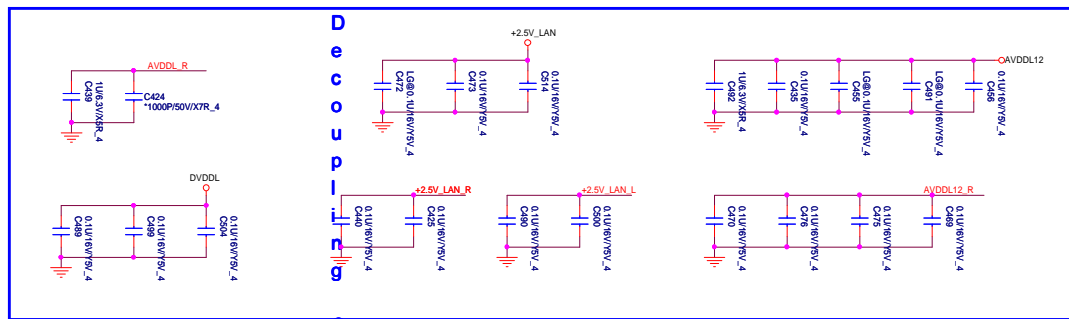
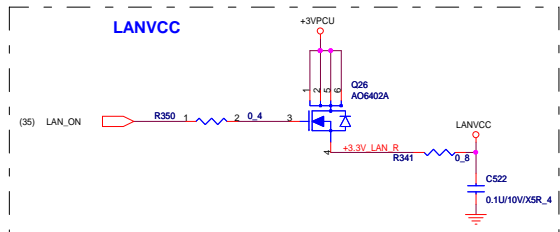
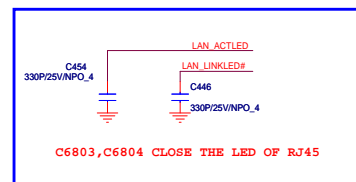
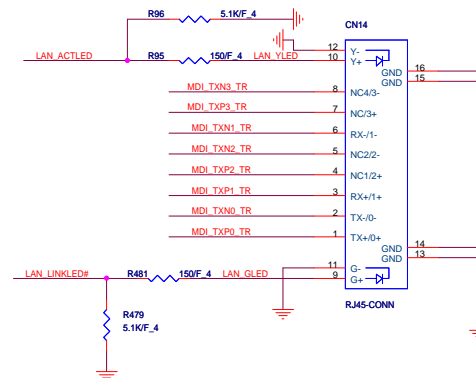
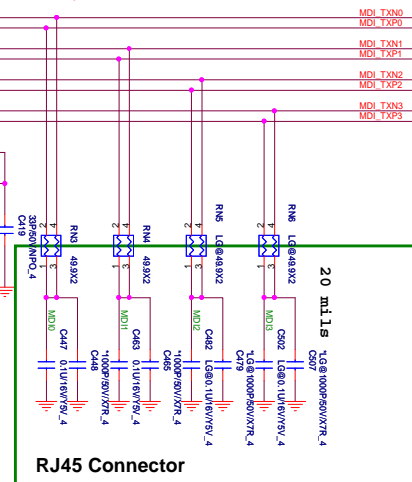
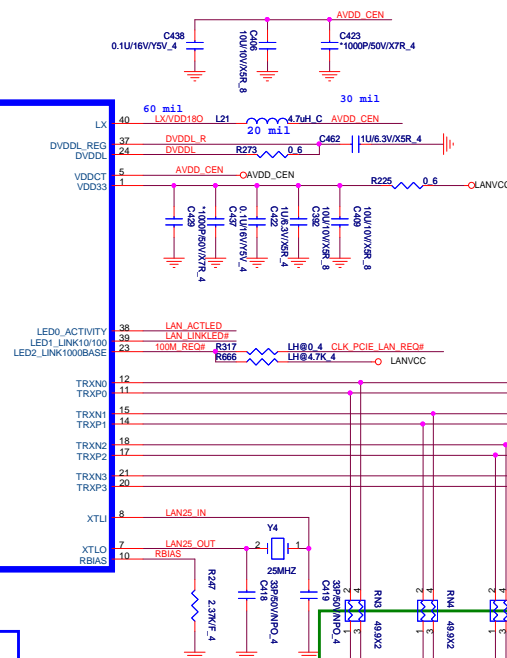
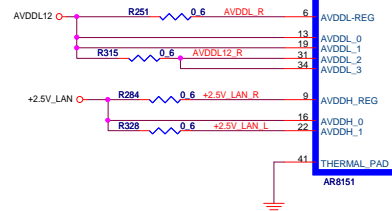
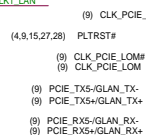
(17)	EXT_CRT_RED	R406	*EV@0 4	CRT R
(17)	EXT_CRT_GREEN	R412	*EV@0 4	CRT G
(17)	EXT_CRT_BLUE	R415	*EV@0 4	CRT B
(17)	EXT_HSYNC_COM	R397	*EV@0 4	HSYNC_COM
(17)	EXT_VSYNC_COM	R394	*EV@0 4	VSYNC_COM
(18)	EXT_CRT_DDCCLK	R386	*EV@0 4	CRT DDCCLK
(18)	EXT_CRT_DDCDATA	R391	*EV@0 4	CRT DDCDATA

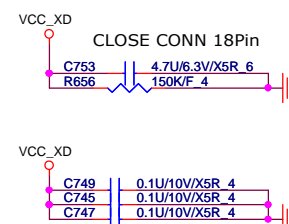
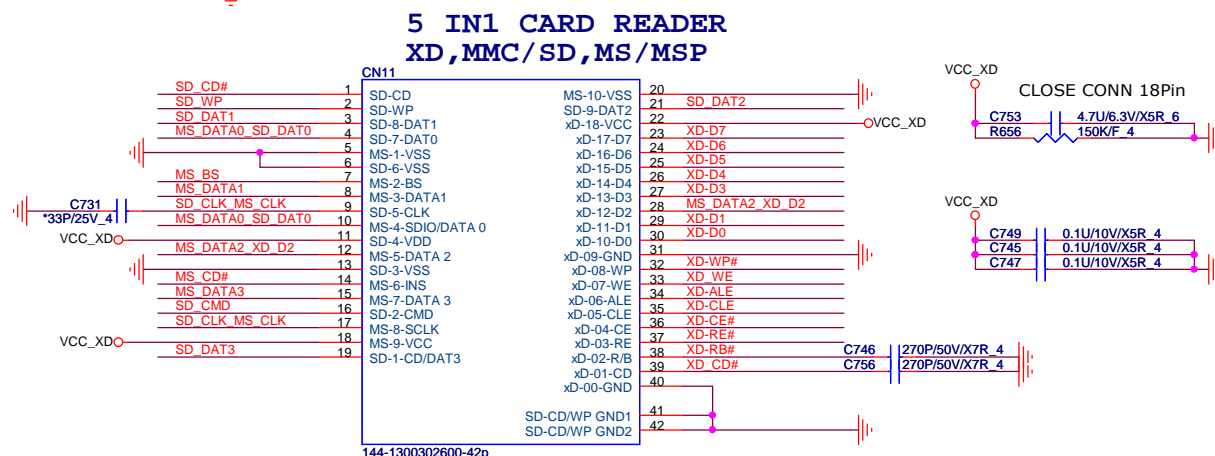
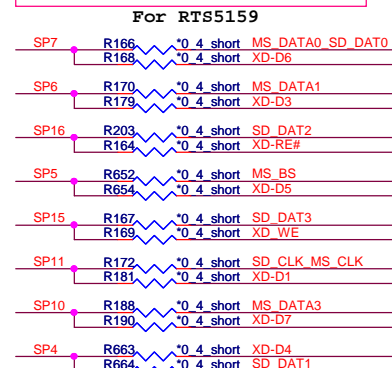
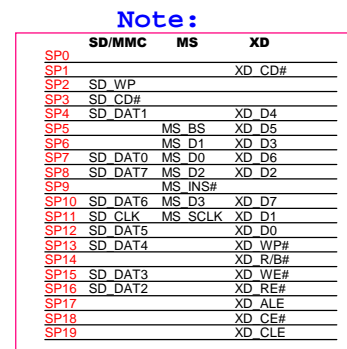
Signals		<i>PDT</i>		
EMI0	<b>Rh</b>	NC	NC	NC
EMI1	<b>Ri</b>	NC	NC	NC
ASQ0	<b>Rj</b>	4.7K	NC	NC
ASQ1	<b>Rk</b>	499	1.2K	4.7K



Signals	PS8171	
PIN 4	LEVEL	EQ
PC1/P10	HIGH	1.2db
	MID	2db
	LOW	※ 0db

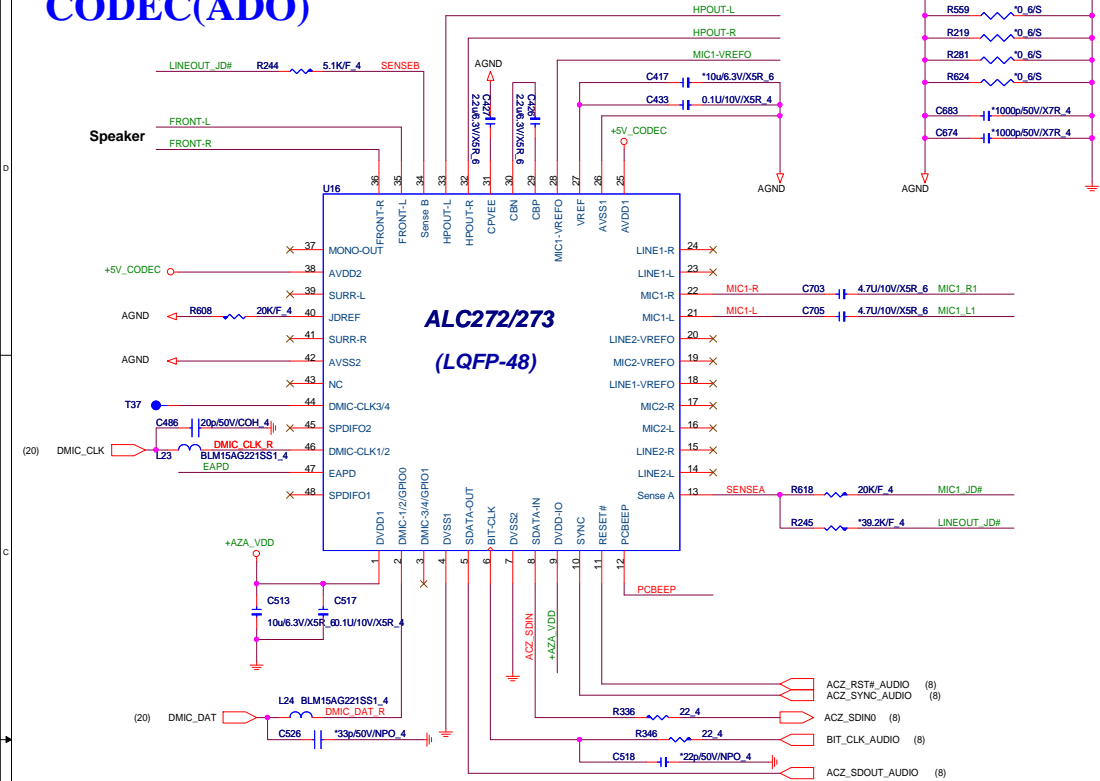




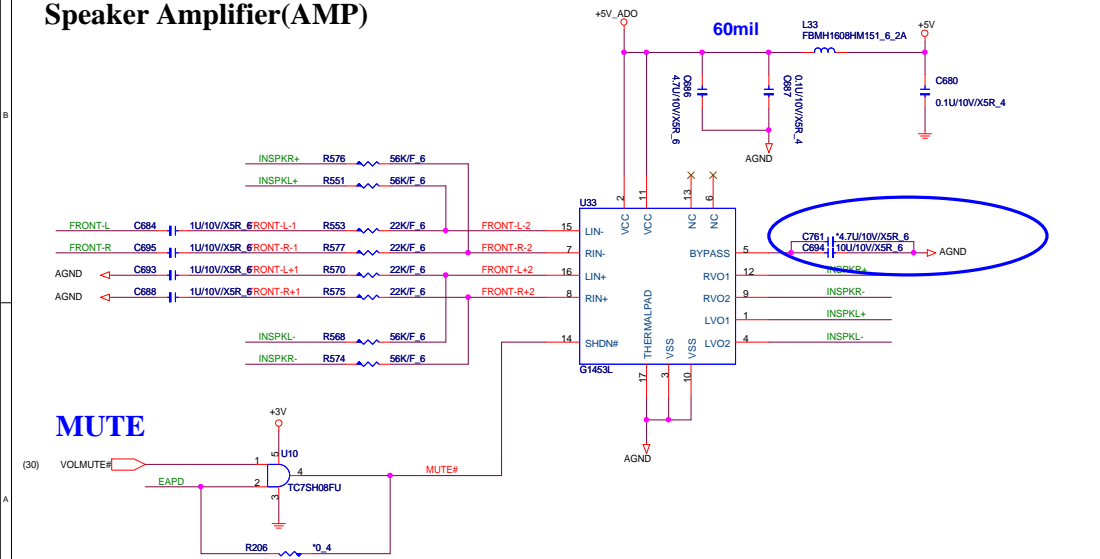


Size B	Document Number <b>CARD READER (Realtek RTS5159)</b>	Rev <b>3A</b>
Date: Thursday, April 08, 2010	Sheet 24	of 42

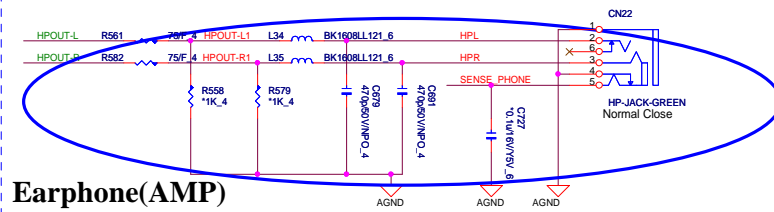
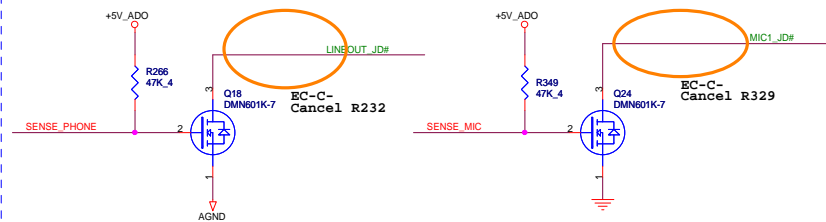
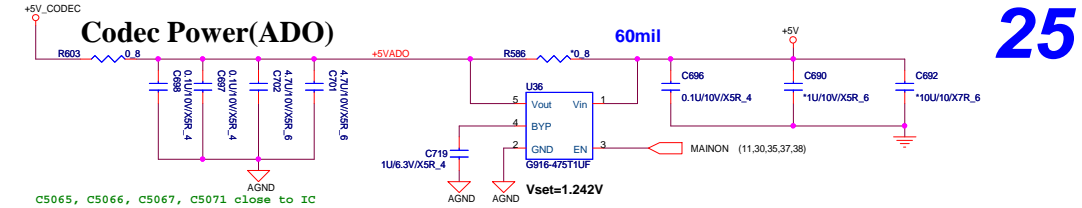
## CODEC(ADO)



## Speaker Amplifier(AMP)

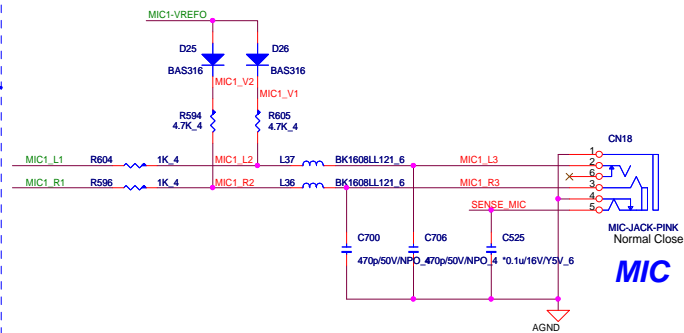


### Codec Power(ADO)



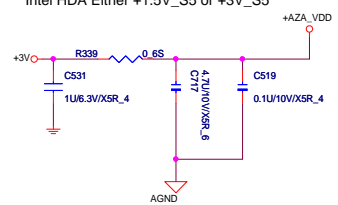
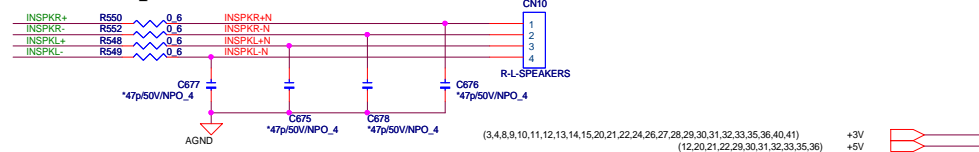
## Earphone(AMP)

## System MIC(AMP)

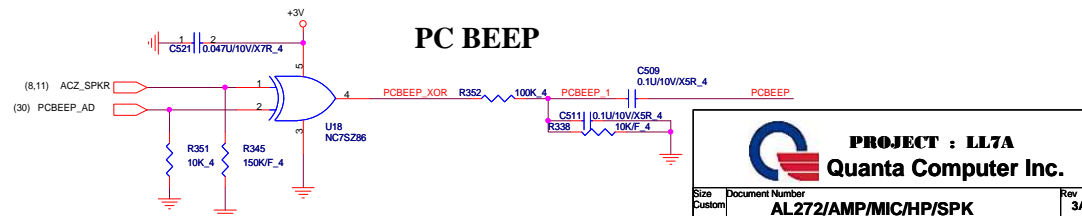


### HDA Power(ADO)

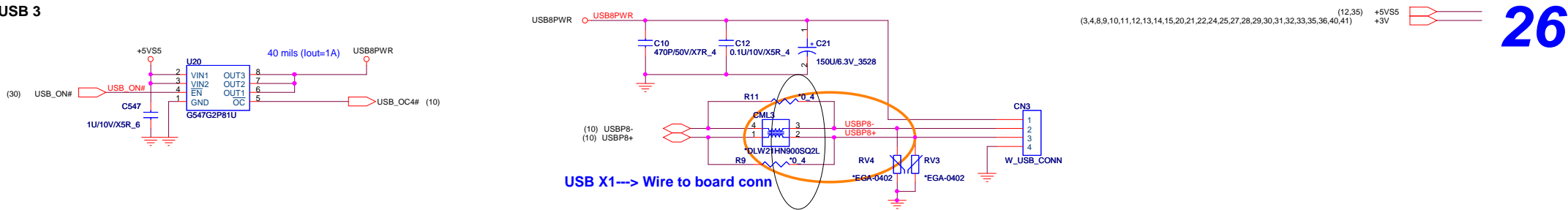
\*Intel HDA Either +1.5V\_S5 or +3V\_S5

**Speaker(AMP)**

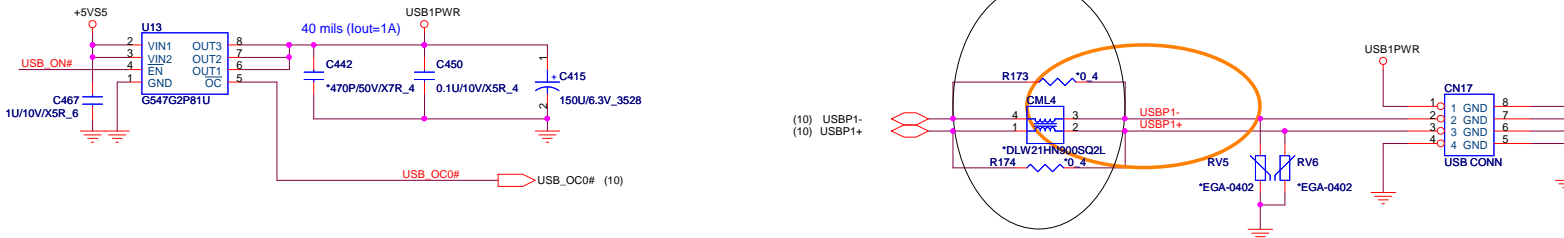
**PC BEEP**



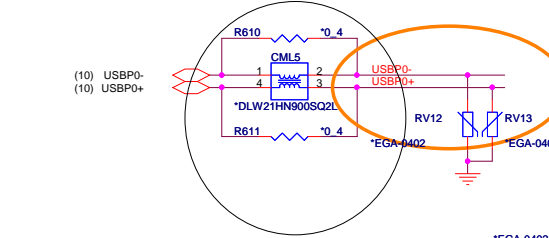
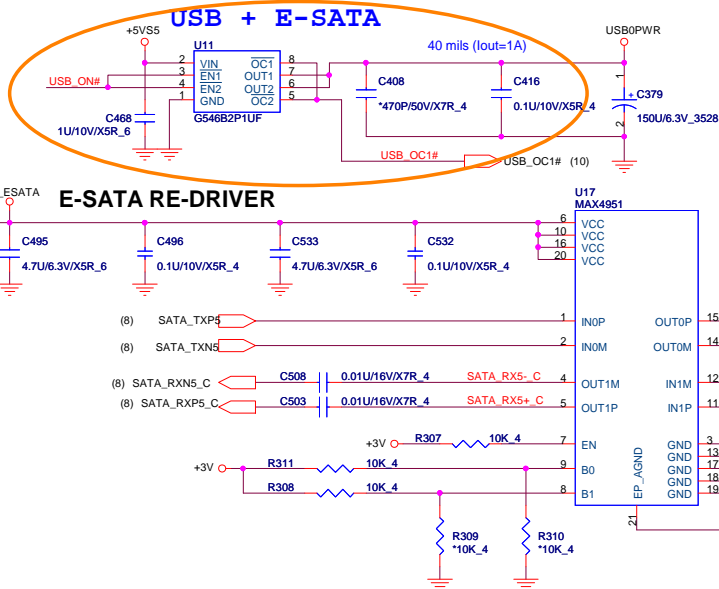
# USB 3



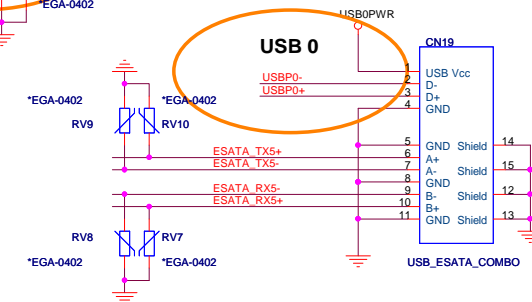
# USB 2



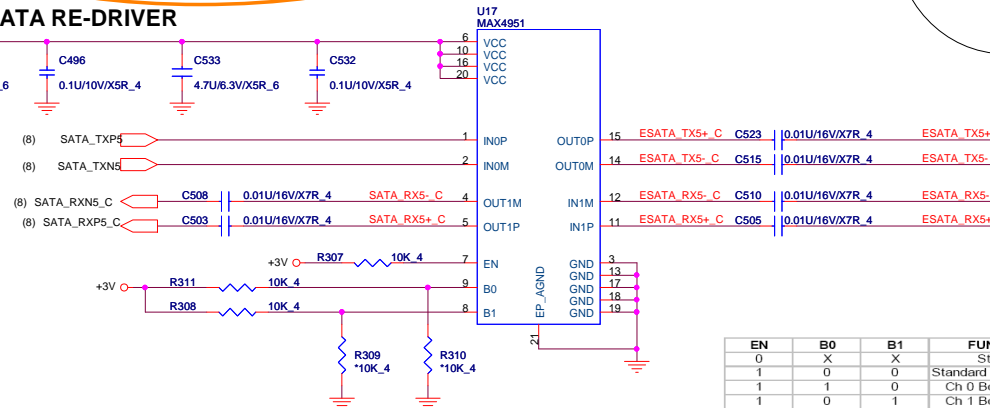
# USB 1



# USB 0



# E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



PROJECT : LL7A  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USBX2/USB+ESATA	3A
Date:	Thursday, April 08, 2010	Sheet 26 of 42

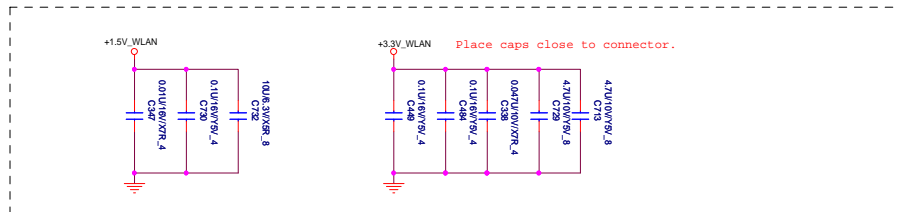
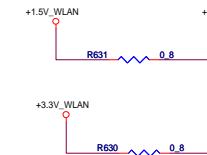
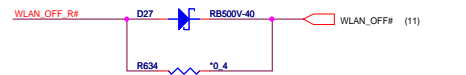
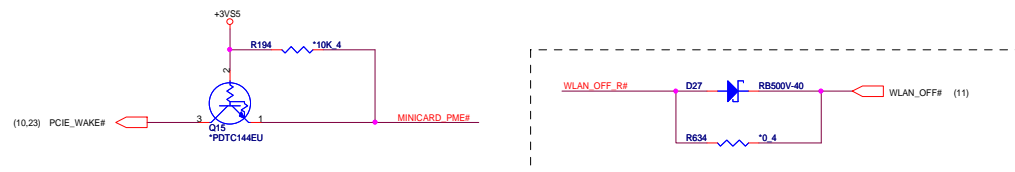
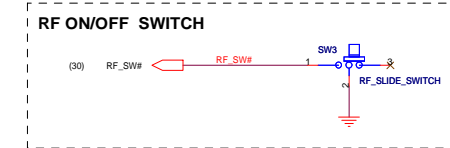
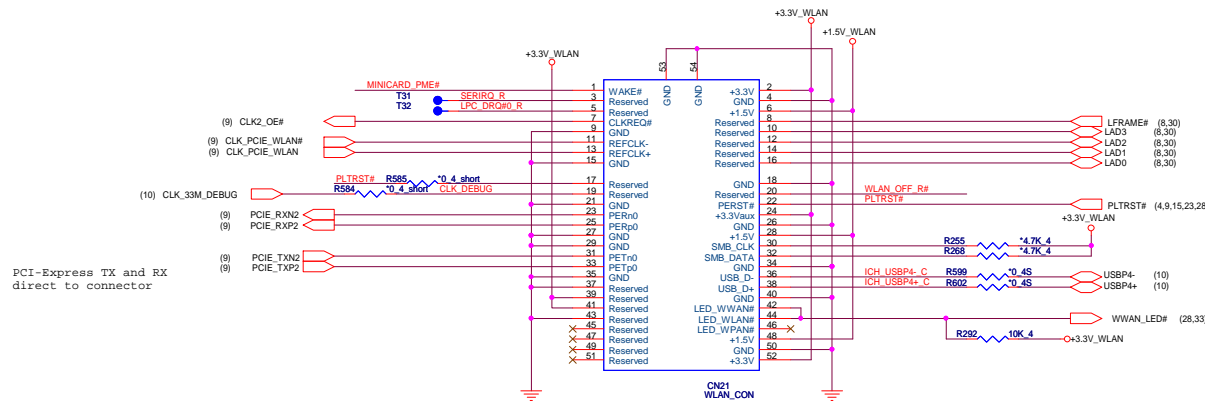


# MiniCard WLAN/WiMAX connector

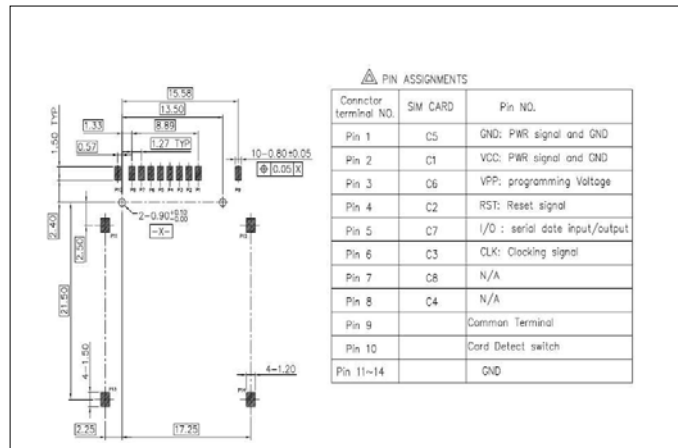
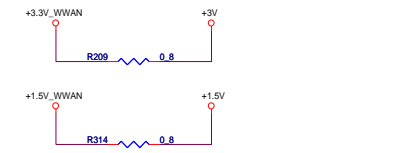
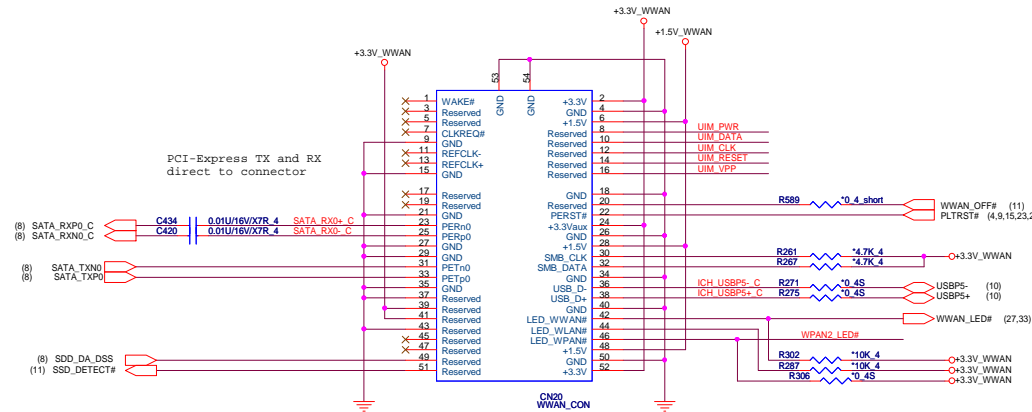
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,28,29,30,31,32,33,35,36,40,41)  
(3,28,37)  
(4,8,9,10,11,12,15,35)

+3V  
+1.5V  
+3V5

27

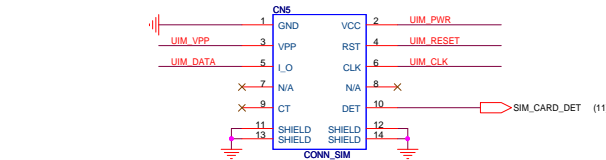


### MiniCard WWAN connector

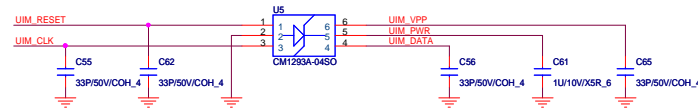


Connector terminal NO.	SIM CARD	Pin NO.
Pin 1	C5	GND: PWR signal and GND
Pin 2	C1	VCC: PWR signal and GND
Pin 3	C6	VPP: programming Voltage
Pin 4	C2	RST: Reset signal
Pin 5	C7	I/O : serial date input/output
Pin 6	C3	CLK: Clocking signal
Pin 7	C8	N/A
Pin 8	C4	N/A
Pin 9		Common Terminal
Pin 10		Card Detect switch
Pin 11-14		GND

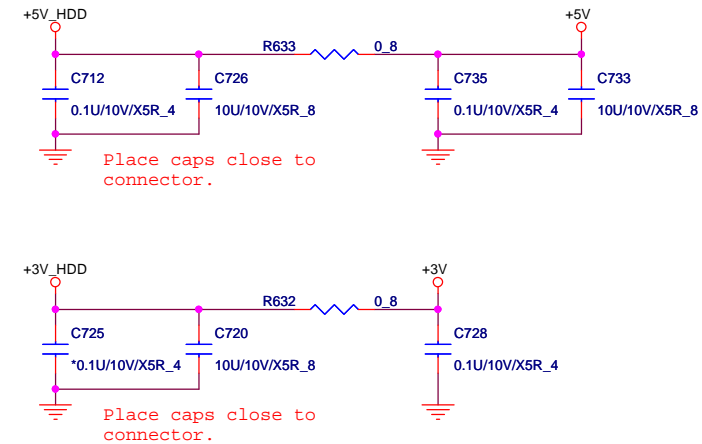
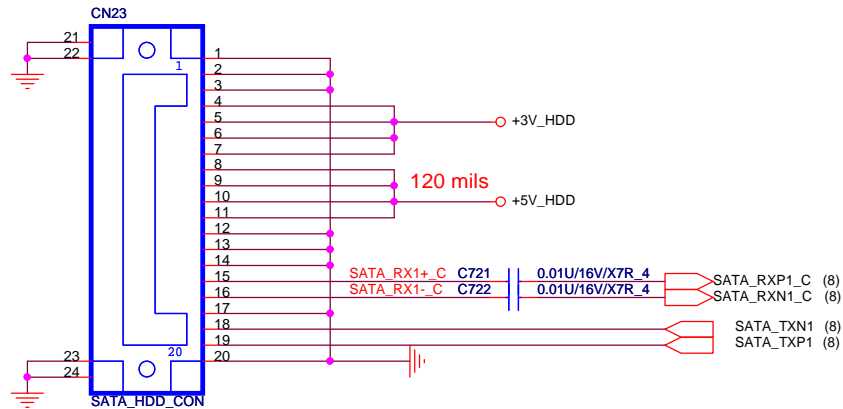
### SIM Card CONN



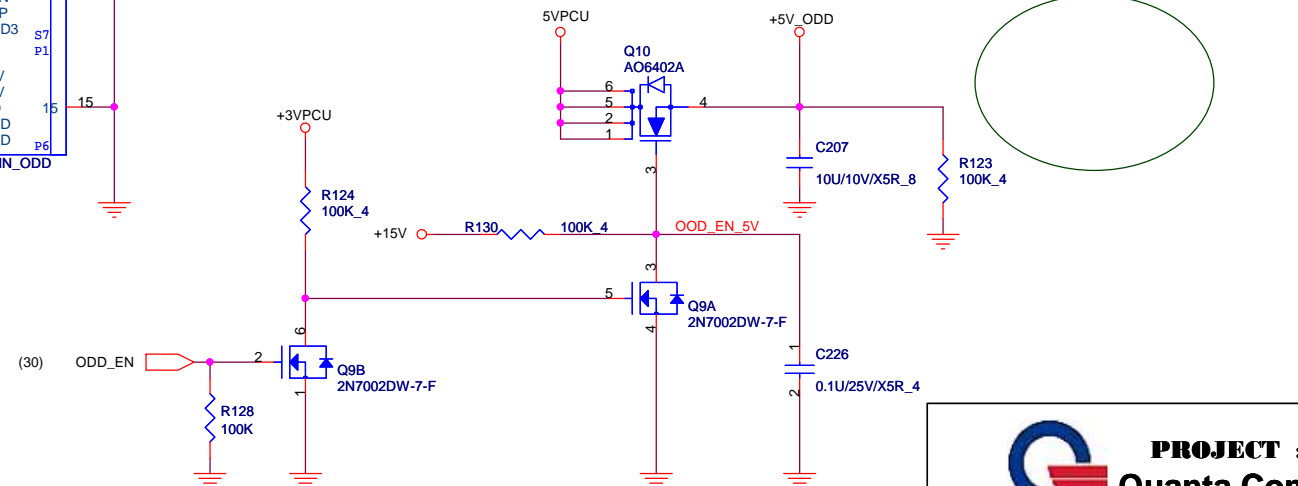
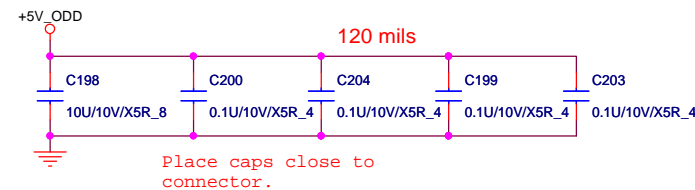
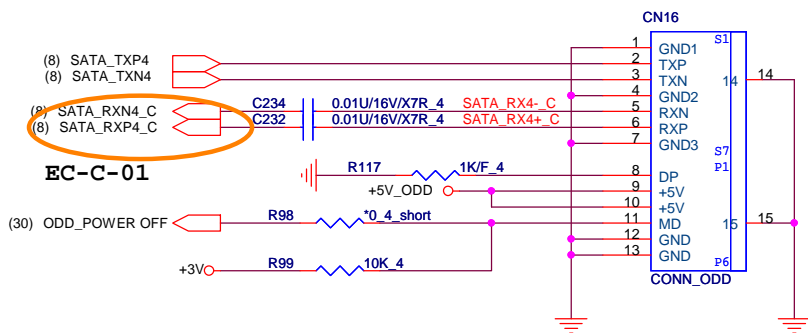
Layout Note:  
UIM\_RESET,UIM\_CLK,UIM\_DATA routing as short as possible



## SATA-HDD CONNECTOR

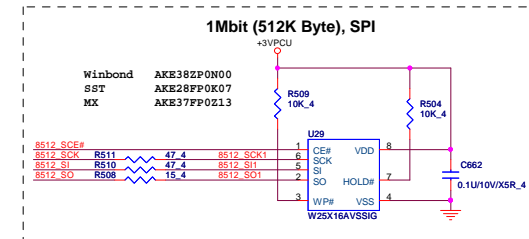


## SATA CD-ROM



**PROJECT : LL7A**  
**Quanta Computer Inc.**

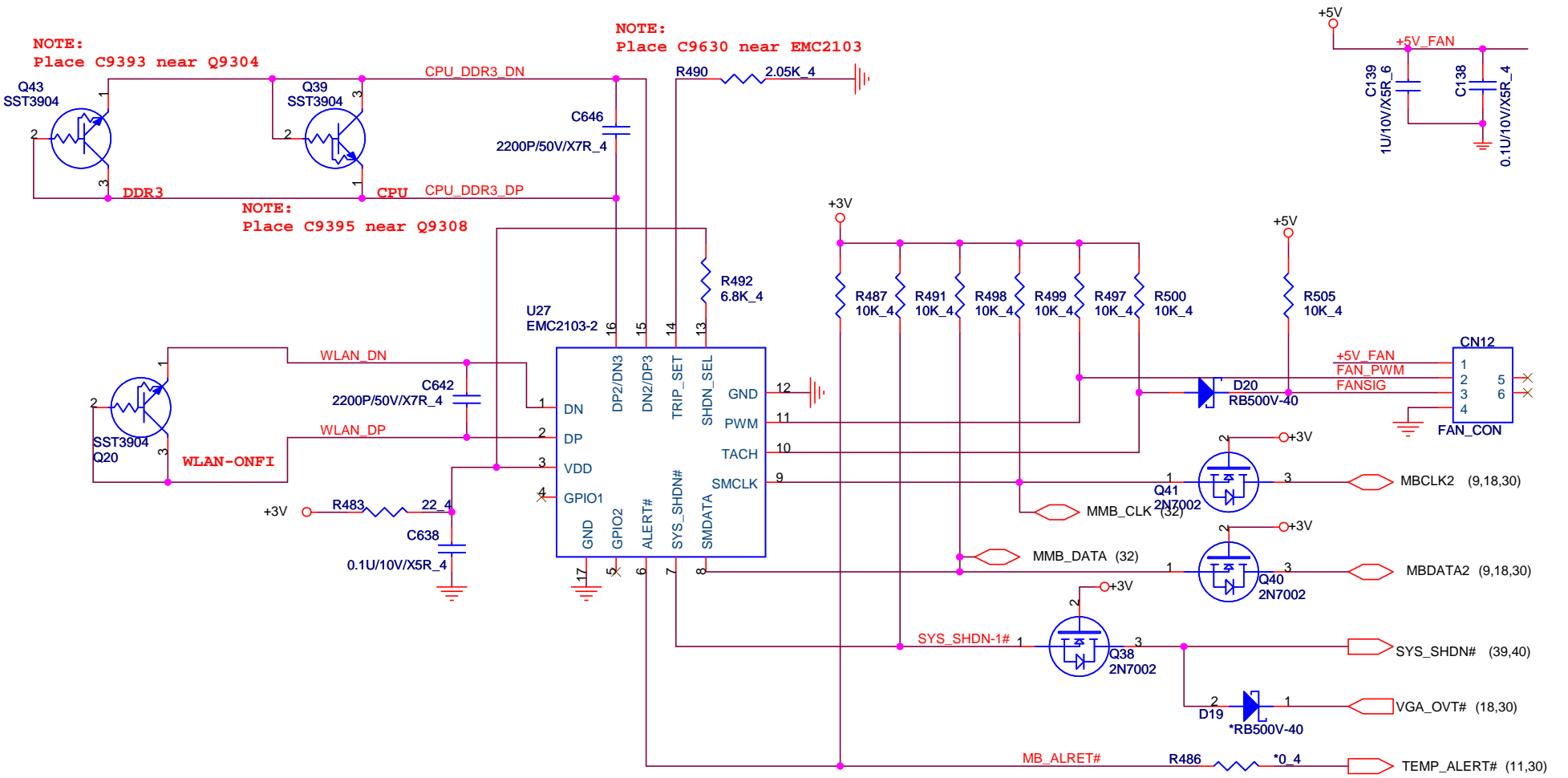
Size	Document Number	Rev
Custom	HDD/ODD	3A
Date:	Thursday, April 08, 2010	Sheet 29 of 42




FAN CONTROL

(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,32,33,35,36,40,41)  
(12,20,21,22,25,29,30,32,33,35,36)

+3V  
+5V

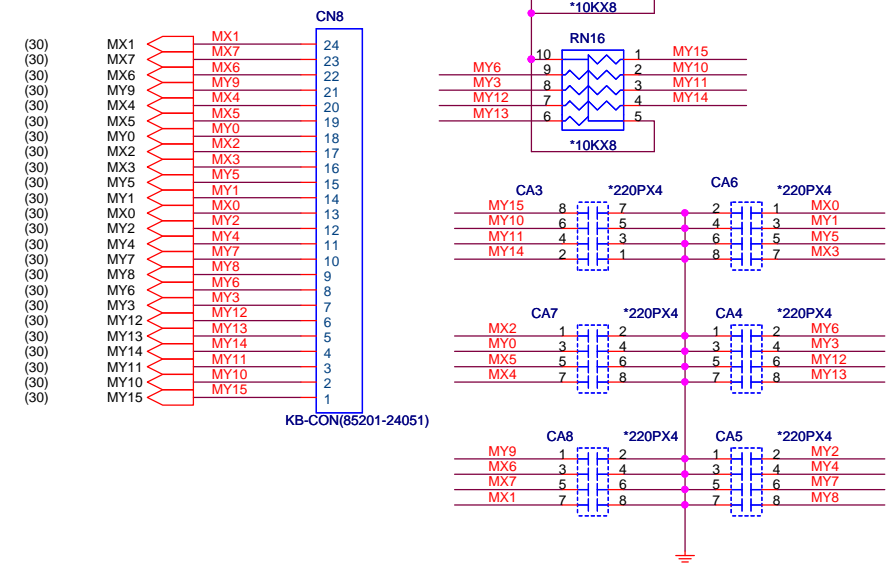




**PROJECT : LL7A**  
**Quanta Computer Inc.**

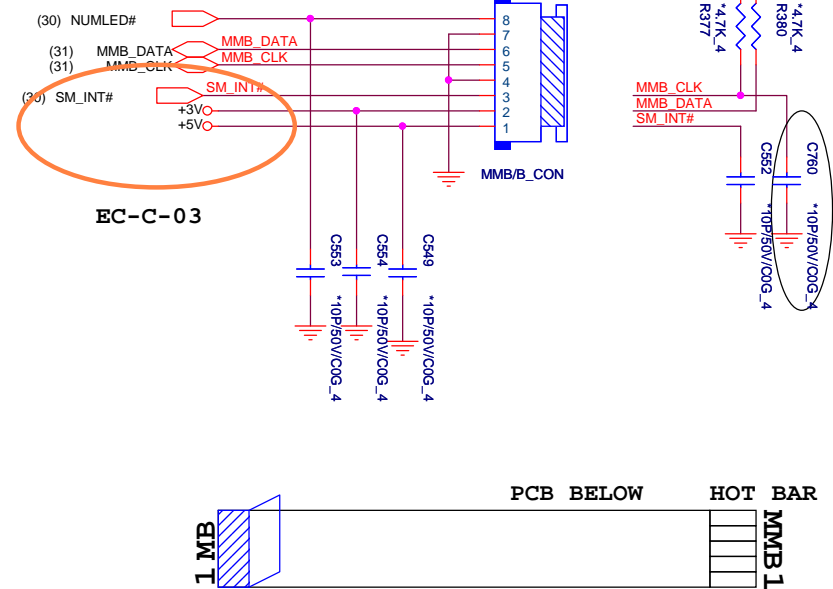
Size	Document Number	Rev
Custom	<b>FAN / THERMAL</b>	<b>1A</b>
Date: Thursday, April 08, 2010		Sheet 31 of 42

## KEYBOARD

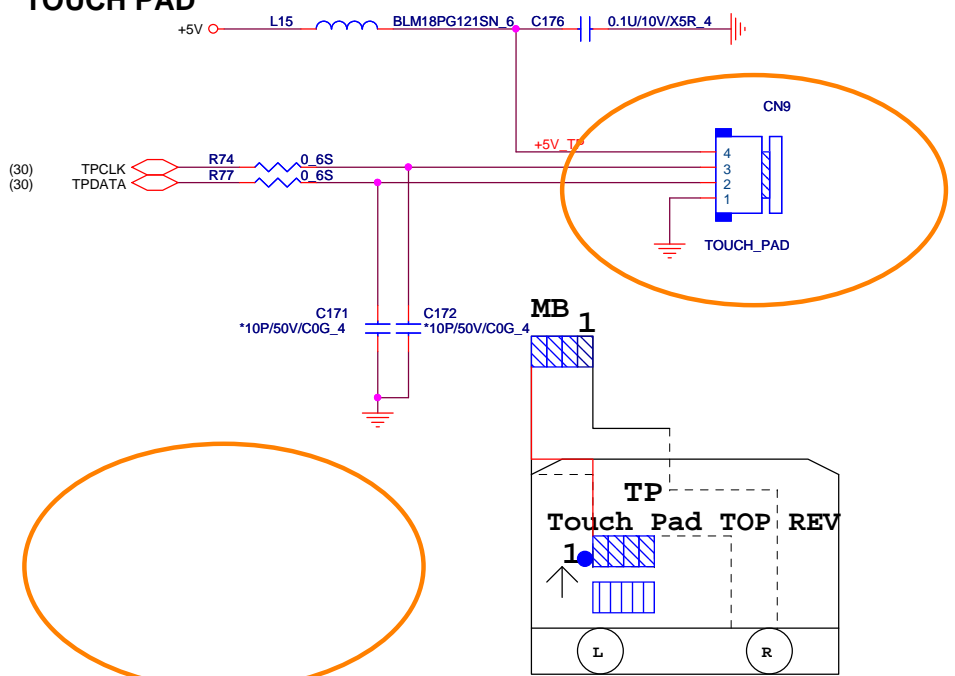


For EMI request

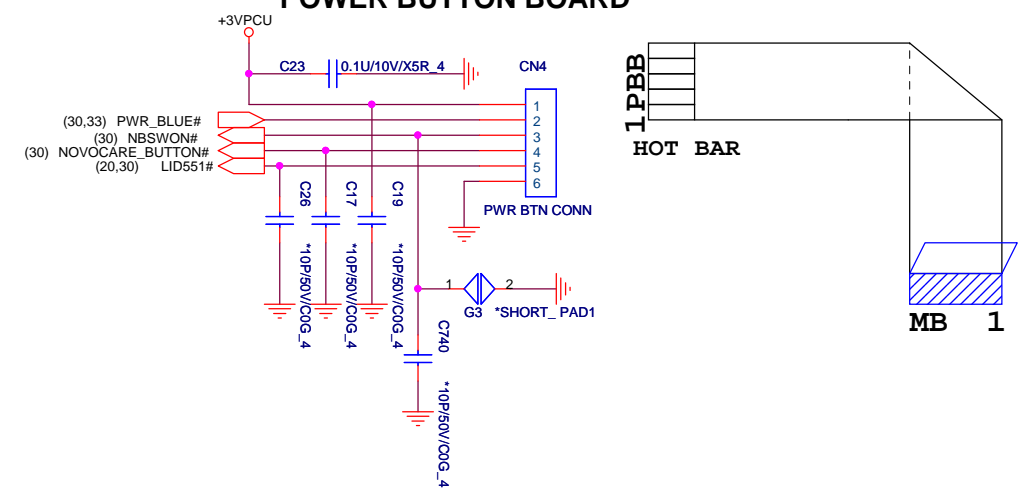
## CAPACITANCE BUTTON BOARD



## TOUCH PAD



## POWER BUTTON BOARD

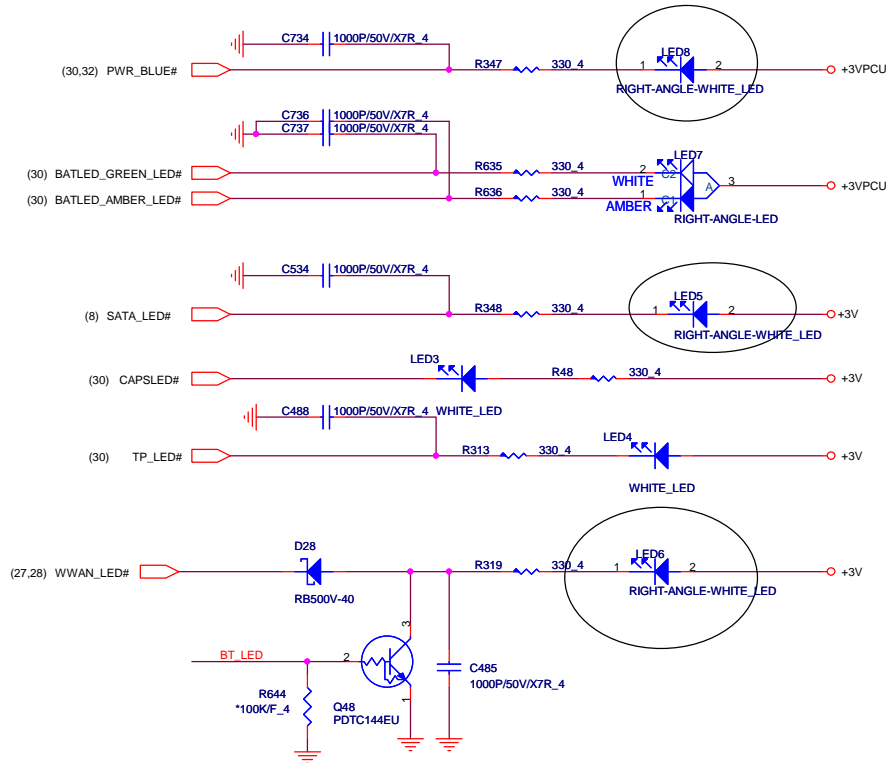


**PROJECT : LL7A**  
**Quanta Computer Inc.**

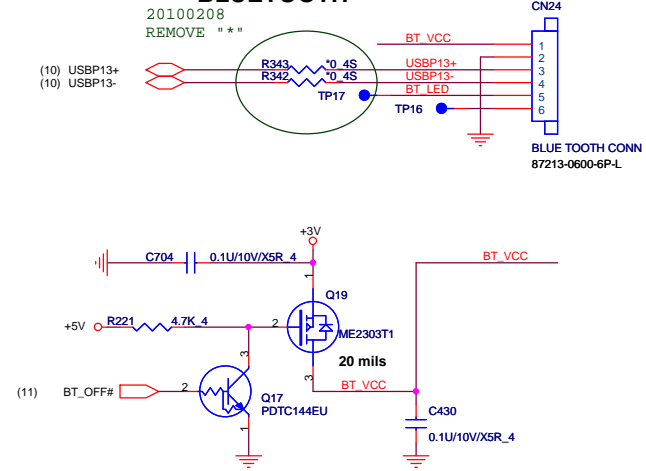


(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,35,36,40,41) +3V  
 (12,20,21,22,25,29,30,31,32,35,36) +5V  
 (8,20,23,29,30,32,35,36,39,41,42) +3VPCU

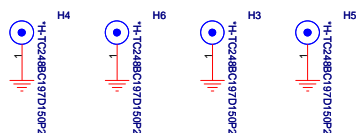
## LED



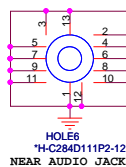
## BLUETOOTH



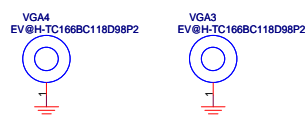
## CPU BKT



## CRT HOLE



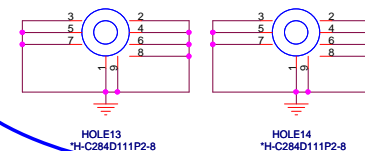
## GPU NUT



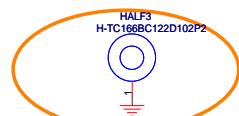
## ODD HOLE



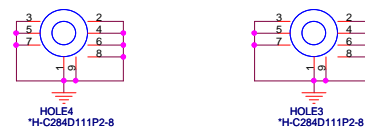
## KEYBOARD HOLE



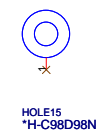
## WLAN nut



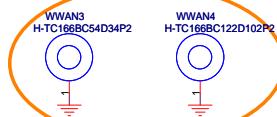
## BATTERY HOLE



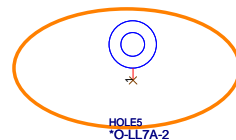
## WLAN CABLE HOLE



## WWAN NUT



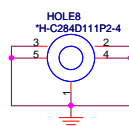
## WLAN CABLE HOLE



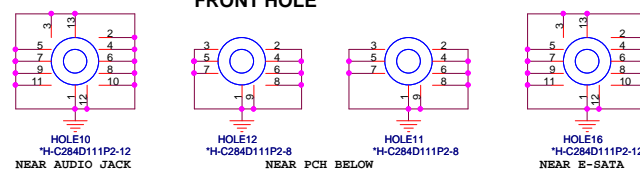
## EMI BATTERY PAD



## DDR 3 HOLE



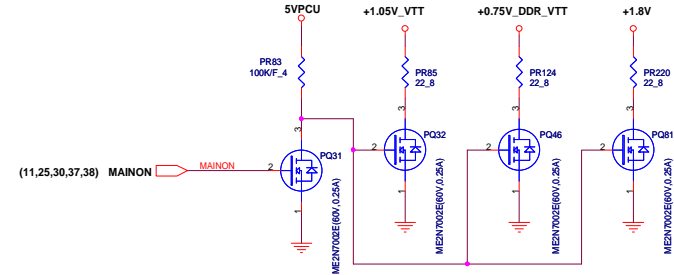
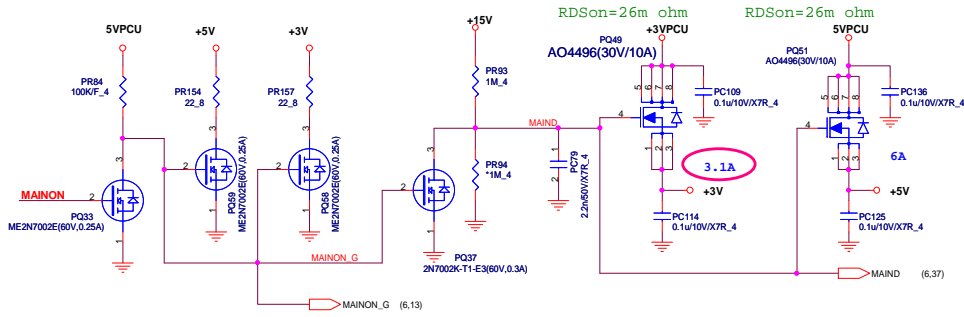
## FRONT HOLE



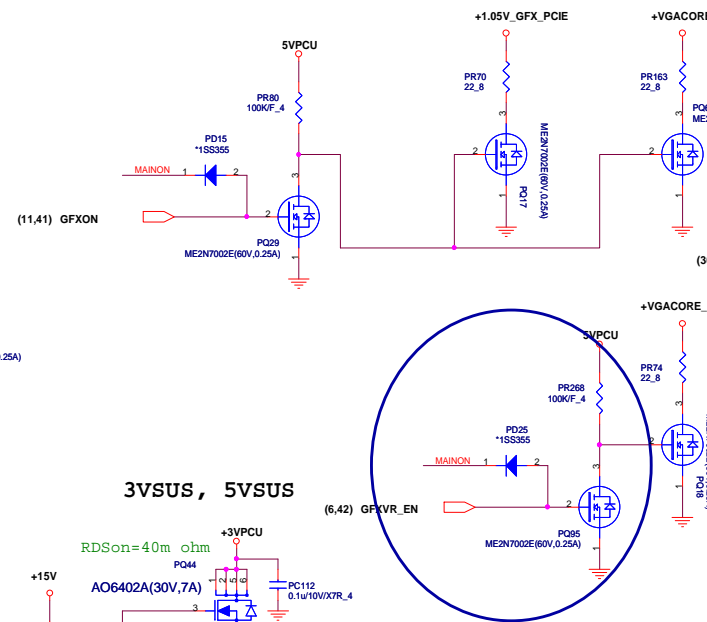
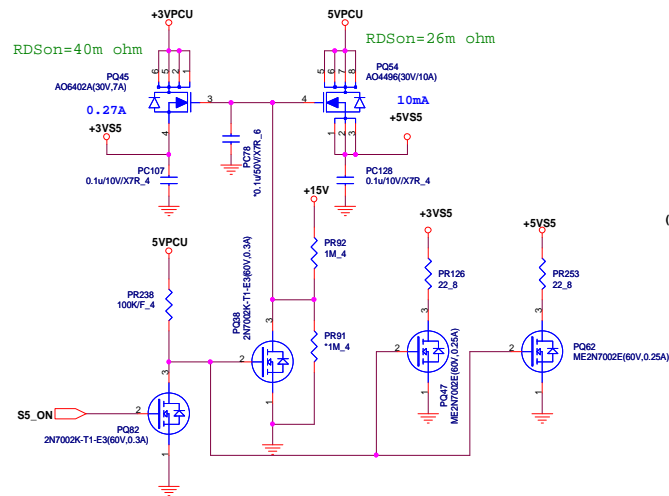
**PROJECT : LL7A**  
**Quanta Computer Inc.**

## DISCHARGE

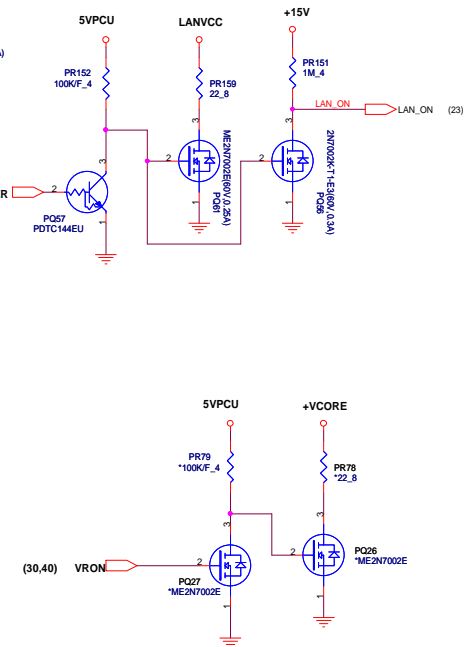
+3V, +5V



3V\_S5, 5V\_S5



LANVCC



3VSUS, 5VSUS

